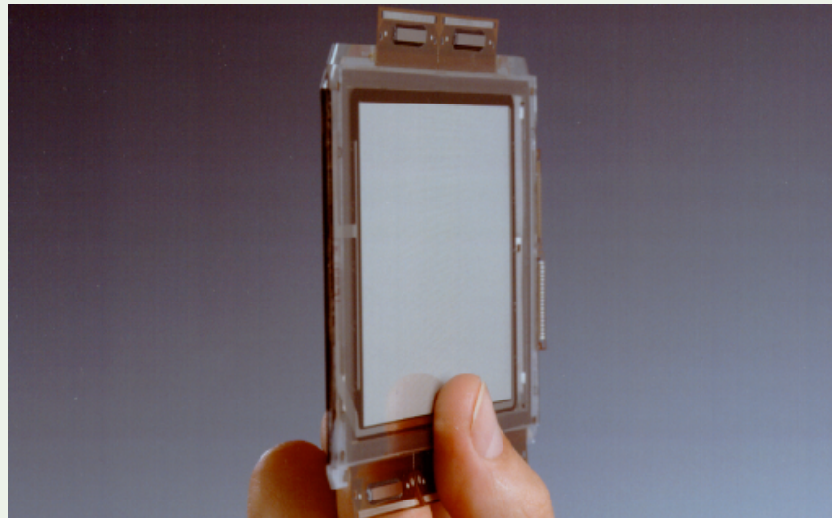


Field-Emission Flat Panel Display Manufacturing



Daniel M. Dobkin

July 2005

Outline

- Introduction to Field Emission displays
 - terminology
 - design choices
 - performance specifications
- Overview of tube components
- Cathode fabrication
- Faceplate fabrication
- Tube assembly

Technology Driving Forces

■ Semiconductors:

- Feature size: smaller is better
- Chip size: smaller is better
- Cost: driven by feature/chip size and complexity

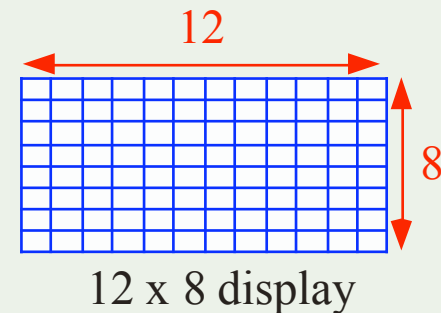
■ Displays:

- Feature size: doesn't matter much (limited by human vision)
- Display size: bigger is better
- Cost: driven by number of display pixels

Display Terminology

(horizontal pixels x vertical pixels)

EWS	2000x2000
UXGA	1600x1200
SXGA	1280x1024
XGA	1024x768
SVGA	800x600
VGA	640x480
QVGA	320x240



Processed panel sizes:

Generation 1: 300 x 400 mm late 80's

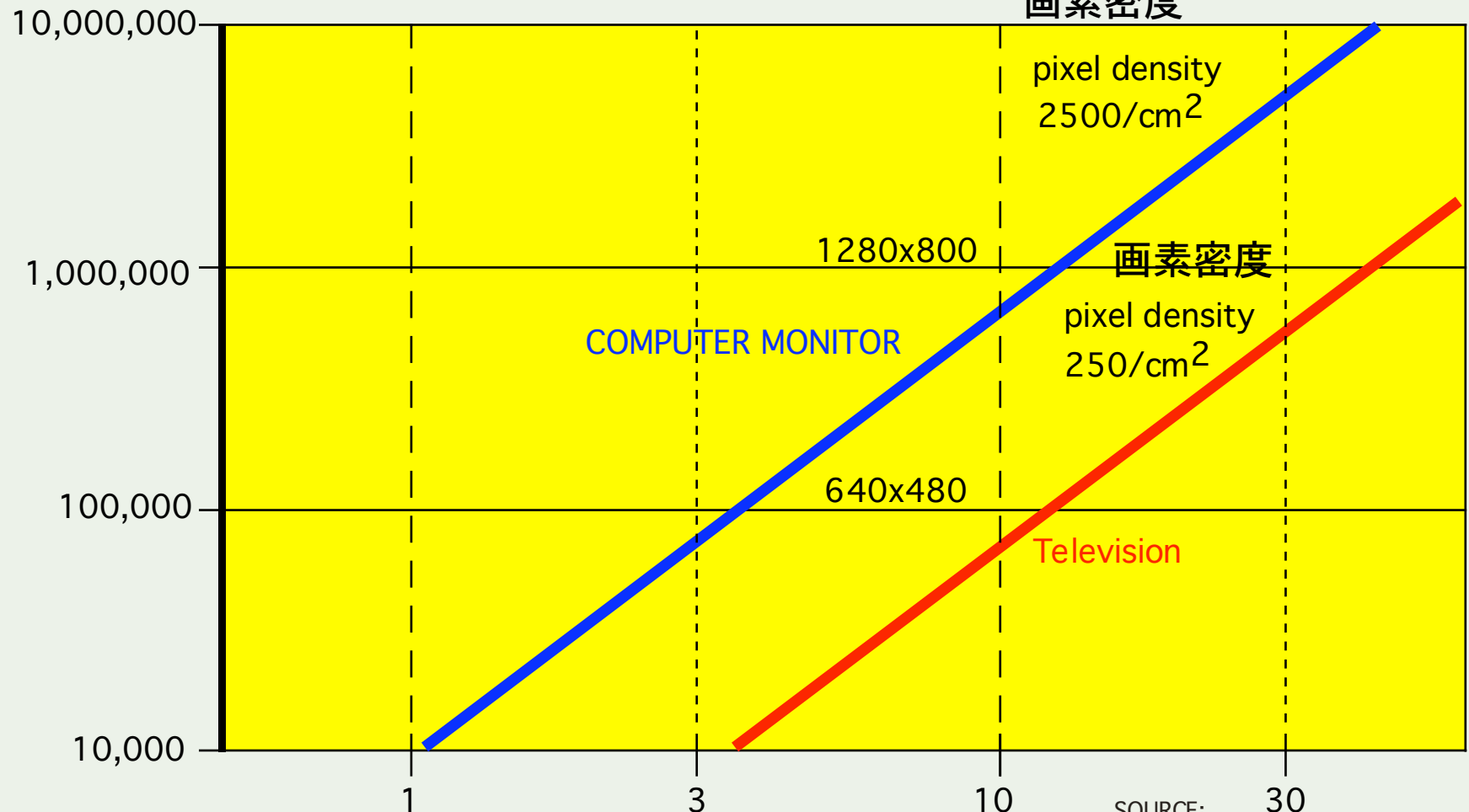
Generation 2: 400 x 500 mm early 90's

Generation 3: 550 x 650 mm late 90's

Today: Generation 7-8 (2 meters square)

Information Content of a Display

Number of Pixels



Display Diagonal (inch)

対角線

SOURCE:
"Liquid Crystal Flat Panel Displays"
W. O'Mara used by permission of the author

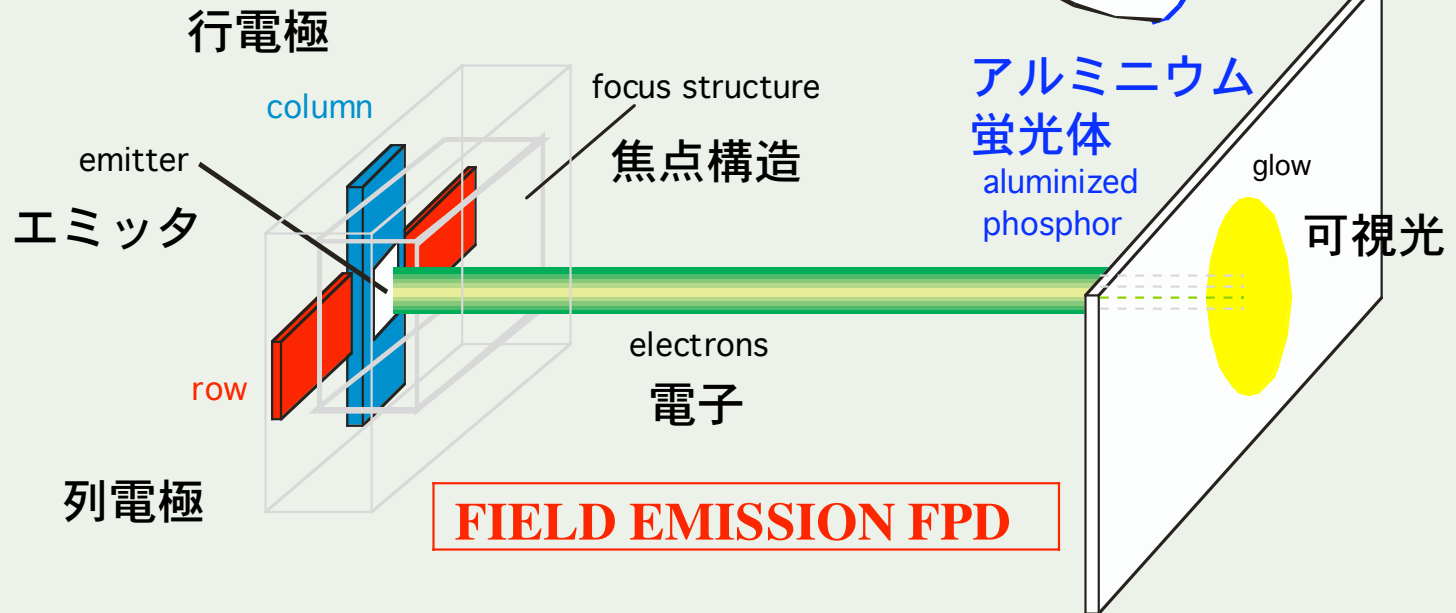
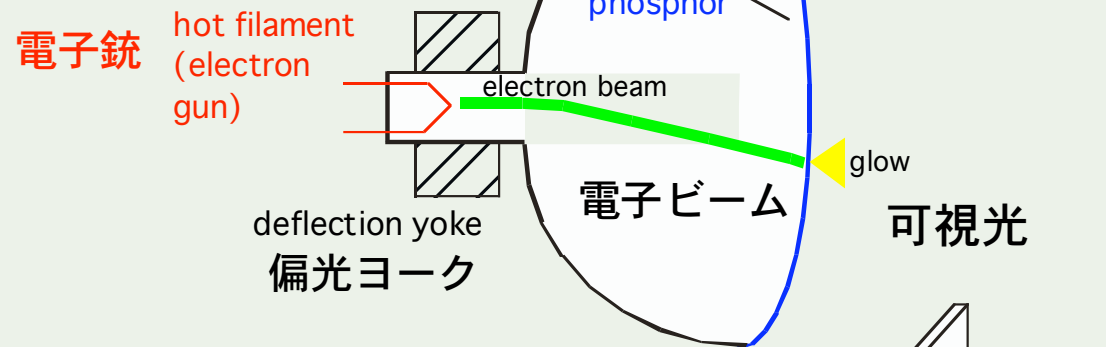
Field Emission Flat Panel Display (pixel)

■ Start with a CRT and squeeze...

Elements of a CRT:

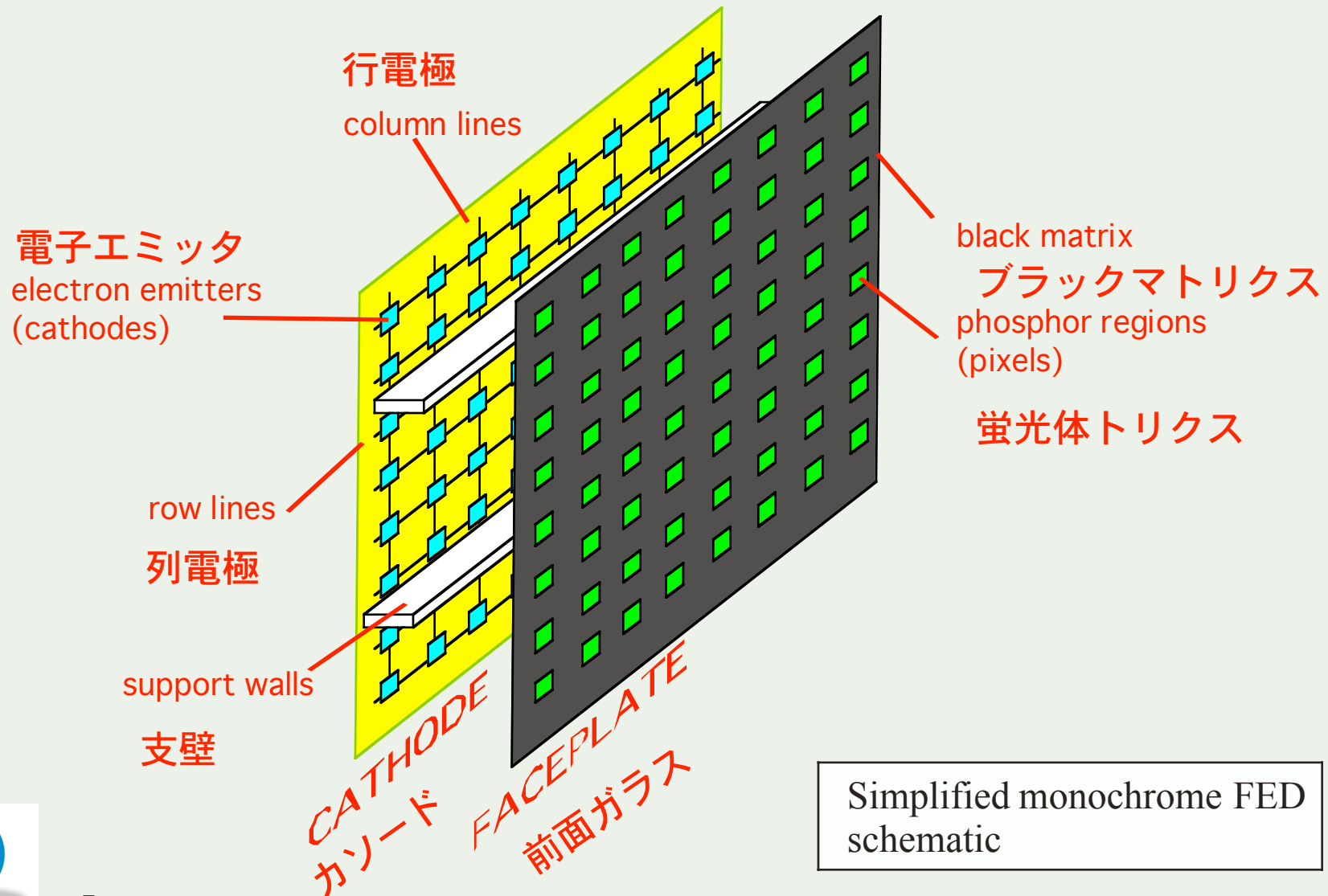
- emit electrons
- form and direct beam
- excite phosphor

CONVENTIONAL



Field Emission Flat Panel Display (matrix)

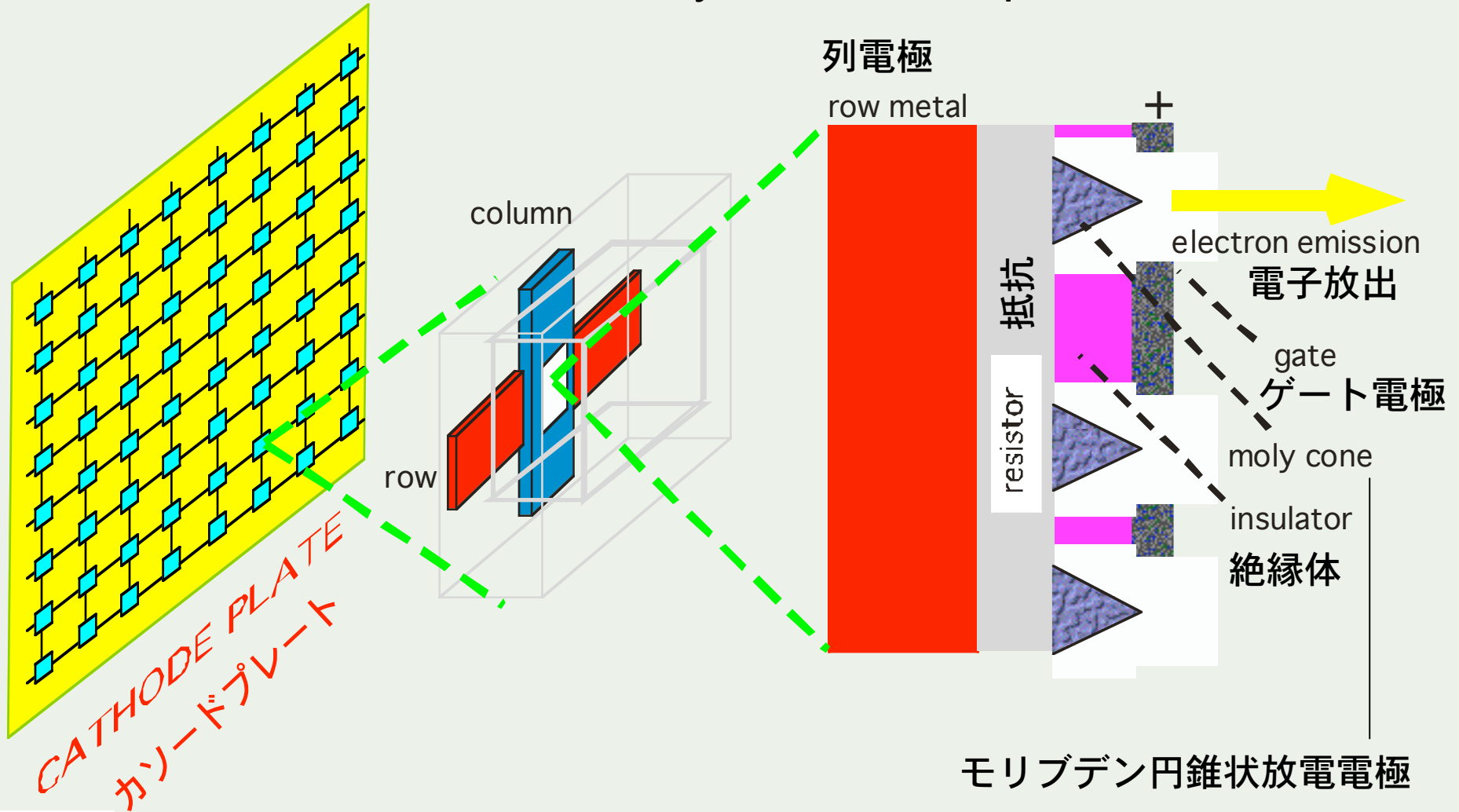
- Matched arrays of emitters and phosphors...



Simplified monochrome FED schematic

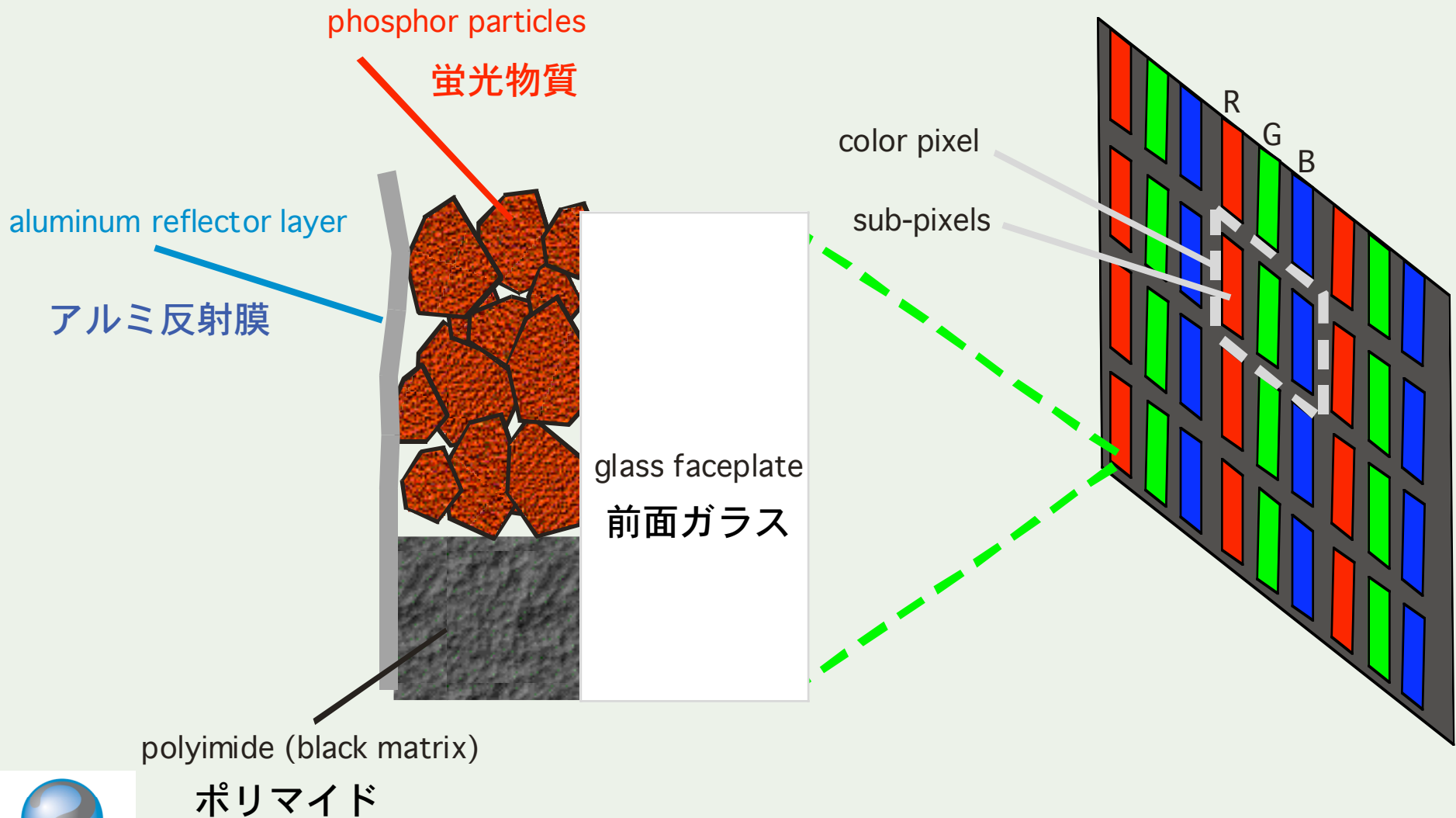
Emitter Detail: Spindt cathodes

- Cone cathodes formed by masked evaporation



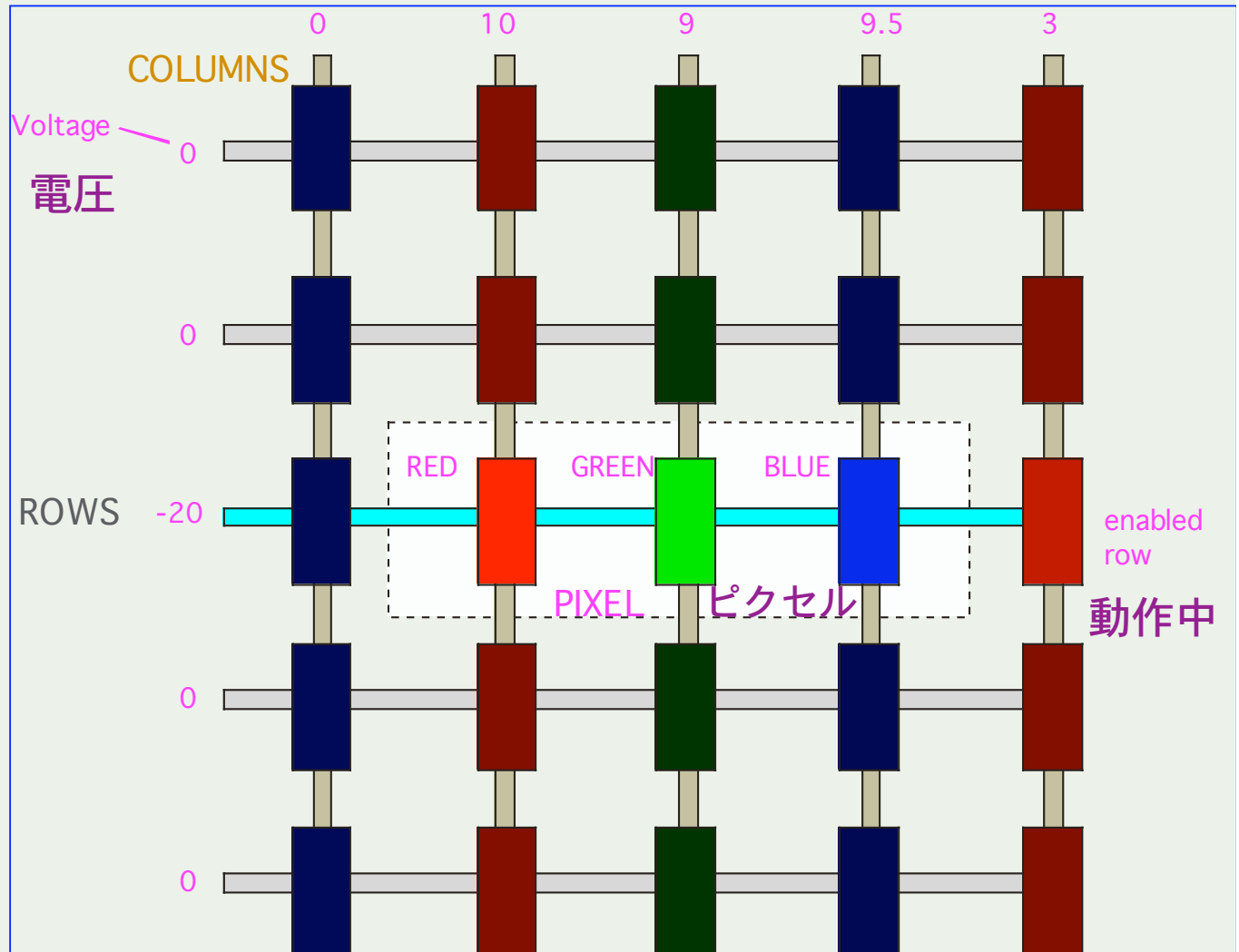
Faceplate Detail: Color phosphors

■ Screen-printed phosphor powders:



Sub-pixel Addressing

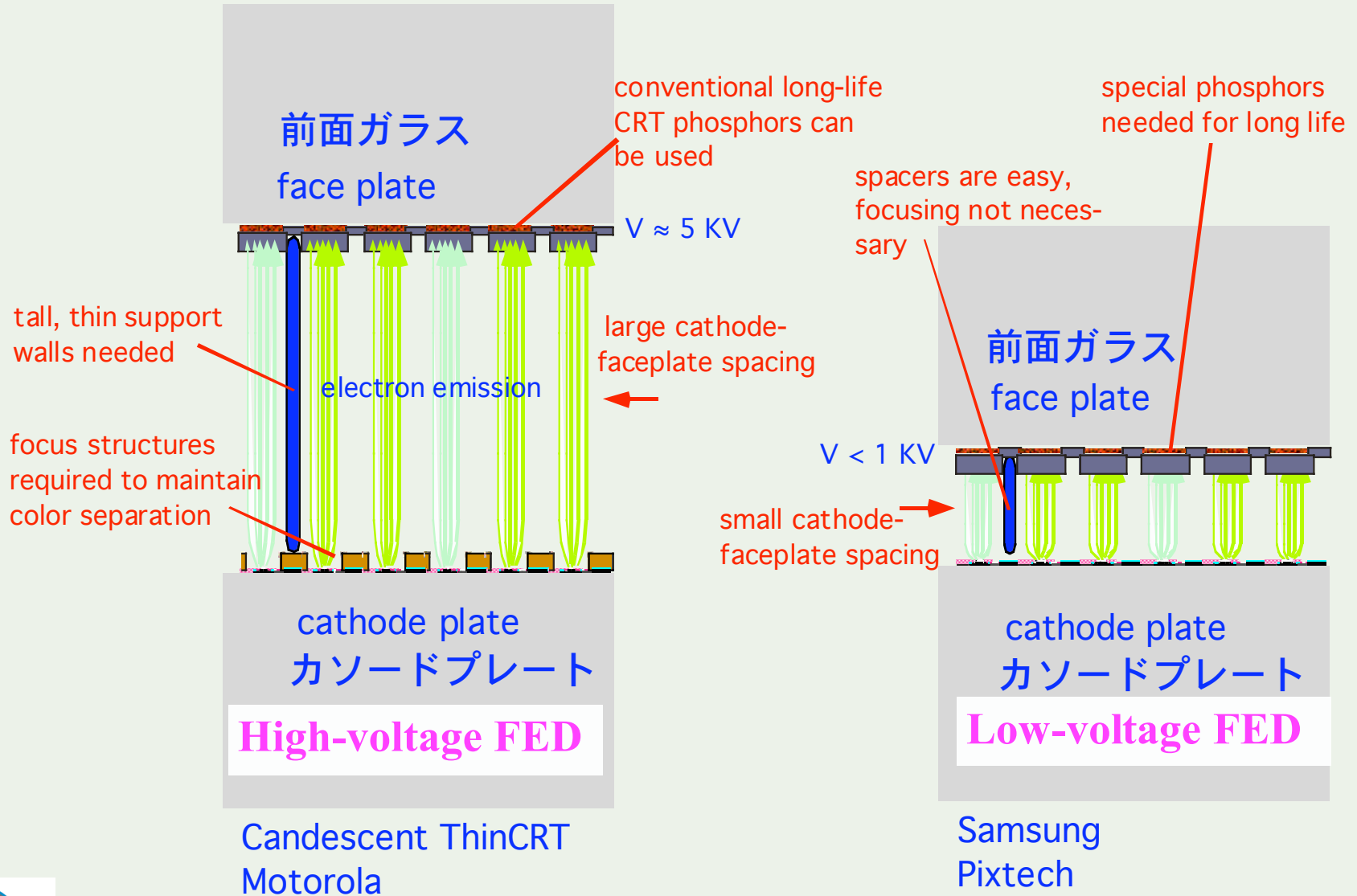
- Highly nonlinear emission-voltage relationship =>
 - cathodes can be used as active devices
 - active matrix not required



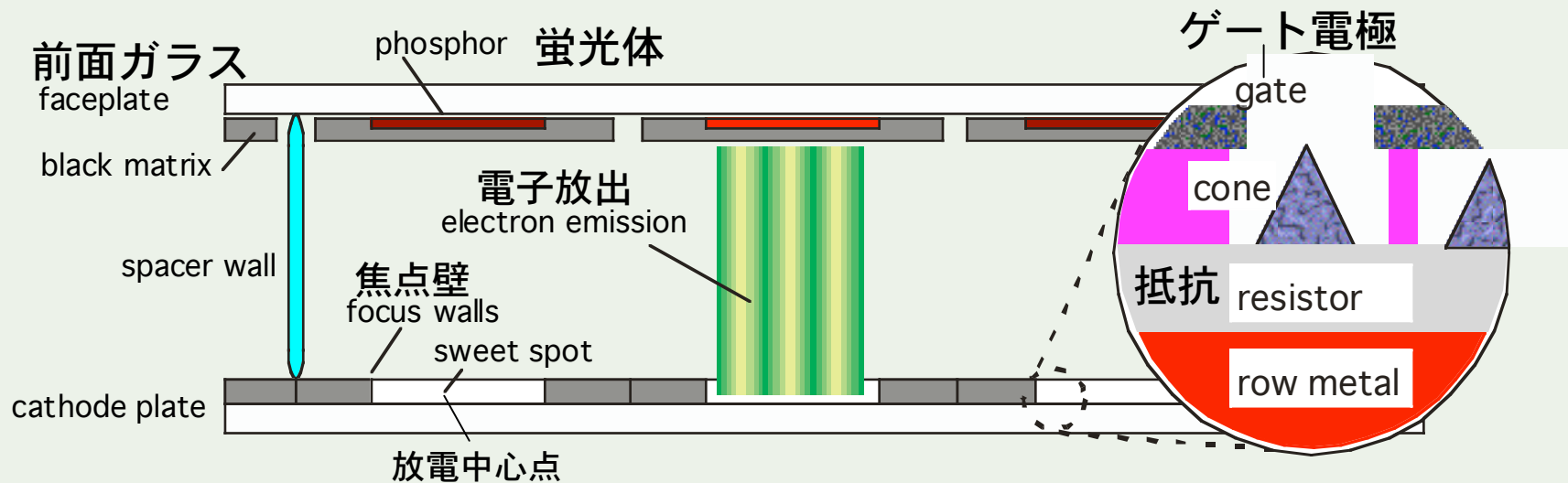
Design Choices

- Faceplate voltage:
 - high voltage = conventional phosphors, high brightness, low coulombic aging BUT high voltage supplies
 - low voltage = special phosphors, aging, but simple power supply
- Cone-gate spacing:
 - tight spacing = low control voltages, simple driver circuits, but hard to build
 - loose spacing = high control voltages but easy fabrication

FED Approaches



FED Cross-Section



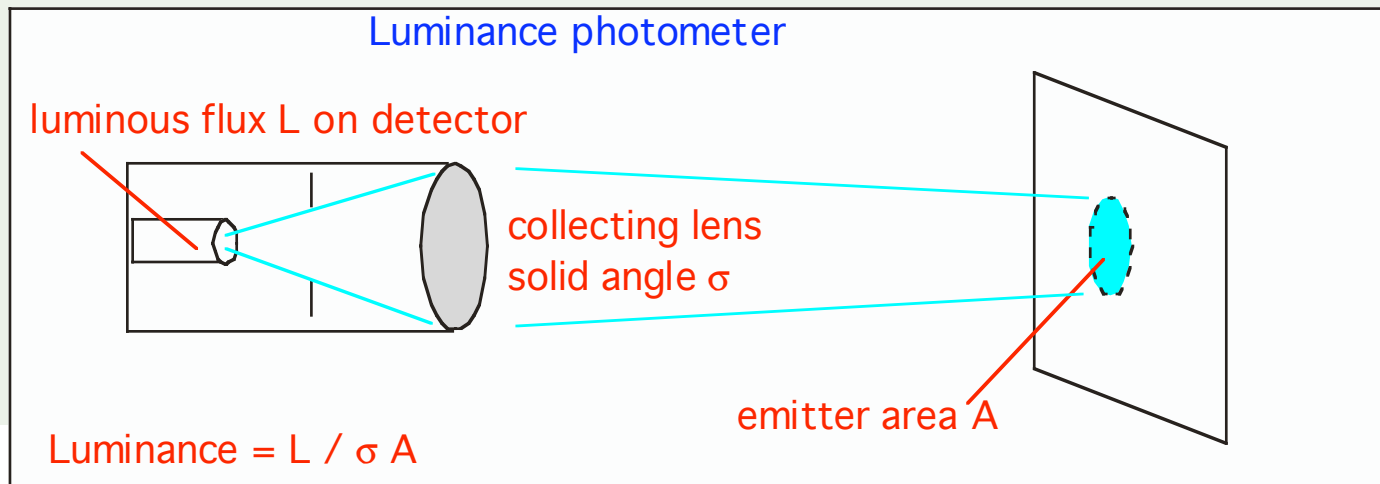
- Roughly to scale
- Fabrication challenges:
 - spacer walls
 - focus structures
 - materials for faceplate / matrix

Display Characterization: Photometry

- Displays have their own terminology...

Name	Description	Unit
Luminous Flux	Light energy (corrected for response of the eye)	lumen
Intensity	Luminous flux per unit solid angle	candela = lumen/steradian
Luminance	Intensity per unit area of emitter	candela/m ² (NIT)
Illuminance	Luminous flux per unit area of receiver	lux = lumen/m ²

1 watt @ 550 nm
= 680 lumens



Display characterization: typical specs

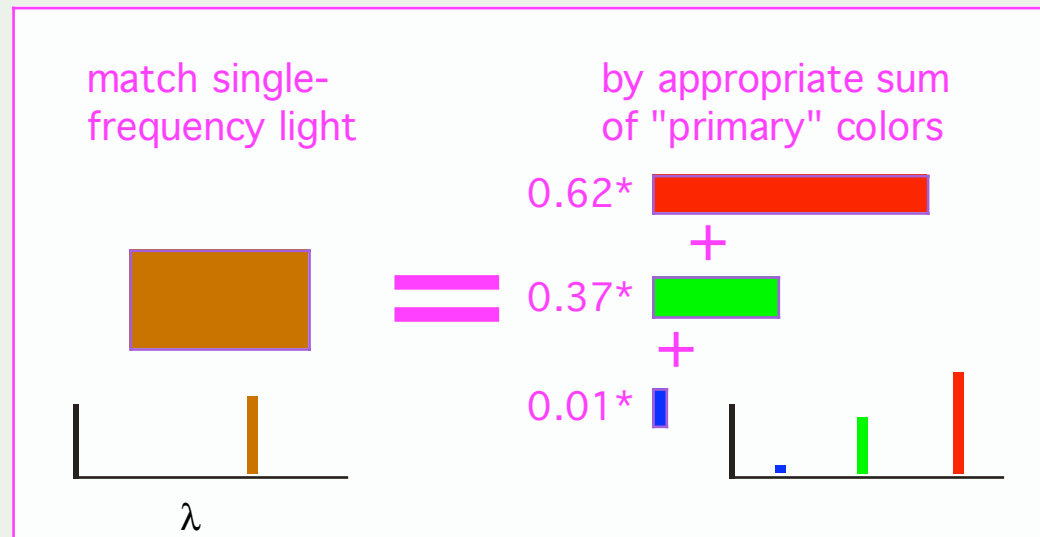
<i>Name</i>	<i>Description</i>	<i>Typical value</i>
power consumption	Voltage * current for image with 67% of full-white	0.7 W @ 70 cd/m ² 0.8 W @ 100 cd/m ²
brightness (luminance)	light/area emitted per steradian of solid angle	100 cd/m ²
brightness uniformity	variation in brightness at various length scales	1% for .3 to 30 mm 3% for 100 mm
video response	time to turn off; determined by phosphor choice	< 5 msec to 10% brightness
viewing angle	measure any parameter (e.g. brightness) vs. angle in plane	170 degrees for emission display
contrast ratio	brightness with all pixels 'on' vs. 'off'	300:1 in dark ambient; >9:1 in brightly lit ambient
defects	missing or dark sub-pixels, rows, or columns	none for usable display (difficult!)
lifetime	on-time to 50% luminance degradation	20,000 hours (target)

Chromaticity and Color

- Human eye does NOT measure spectra directly
 - retina contains three types of cone cells, peak sensitivity at 450, 550, 600 nm
 - brain senses color by relative excitation
 - any visible ‘color’ (power spectral distribution) can be reduced to 3 ‘color coordinates’
- To quantify:
 - define matching functions
 - decompose spectrum into sum of matching functions
 - obtain chromaticity coordinates

Step 1: Find matching functions

- Define “primaries”
 - e.g. Red = 700 nm Green = 546 nm Blue = 436 nm (CIE 1931)
- For monochromatic light, each λ from ≈ 400 -700 nm
 - Vary proportions of R/G/B until visual sensation IDENTICAL for monochromatic light and mixture of primaries
 - Record intensity of each primary vs. wavelength



Result: color matching functions

- Amount of each primary needed to match any given monochromatic illumination

- Note: model is imperfect; “virtual” primaries required to give positive matching function for all wavelengths as shown here.

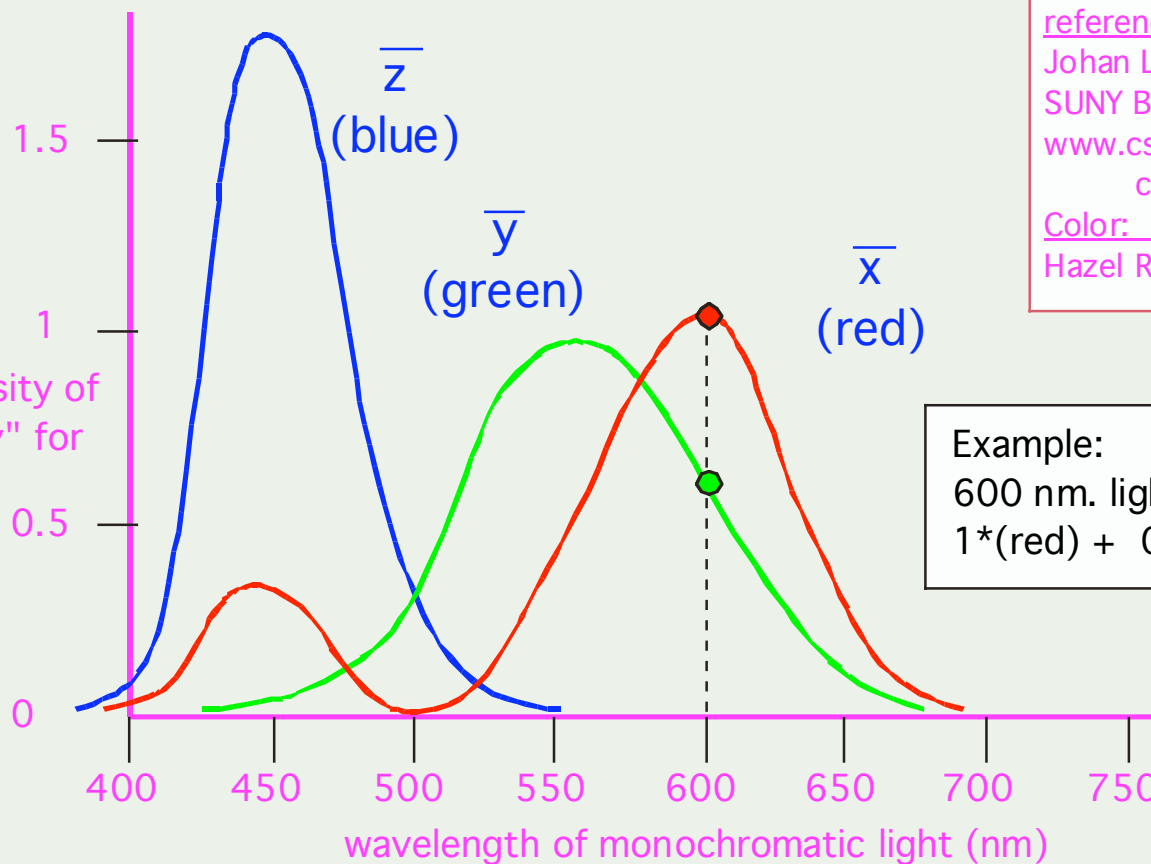
references:

Johan Lamnens Ph.D. Thesis
SUNY Buffalo, 1994

www.cs.buffalo.edu/pub/colornaming/diss

[Color: Why the World Isn't Grey](#),
Hazel Rossotti, Princeton 1983

relative intensity of
each "primary" for
match



Example:

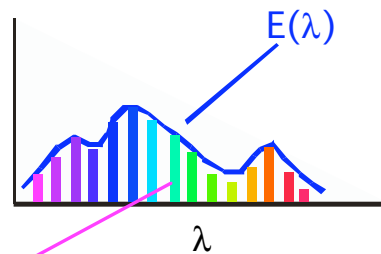
600 nm. light \approx

$1 \cdot (\text{red}) + 0.6 \cdot (\text{green}) + 0 \cdot (\text{blue})$

Step 2: Decompose arbitrary spectrum

- Treat arbitrary light as sum of monochromatic segments
- Emulate each monochromatic segment by appropriate combination of primaries

match arbitrary color by decomposing into spectral lines, building each one from R/G/B primaries



$$0.3(R) + 1.3(G) + 0.1(B)$$

$$X = \int E(\lambda) \bar{x}(\lambda) d\lambda$$

$$Y = \int E(\lambda) \bar{y}(\lambda) d\lambda$$

$$Z = \int E(\lambda) \bar{z}(\lambda) d\lambda$$

Weighted sum of primaries for all colors = "Tristimulus value" : brightness of primaries to emulate original spectrum

- Normalize to unit brightness (i.e. capture only color information):

"Chromaticity coordinates"

- Note requirement of unit brightness implies $x+y+z = 1$: only two coordinates actually required, can display on 2D graph

$$x = \frac{X}{X + Y + Z}$$

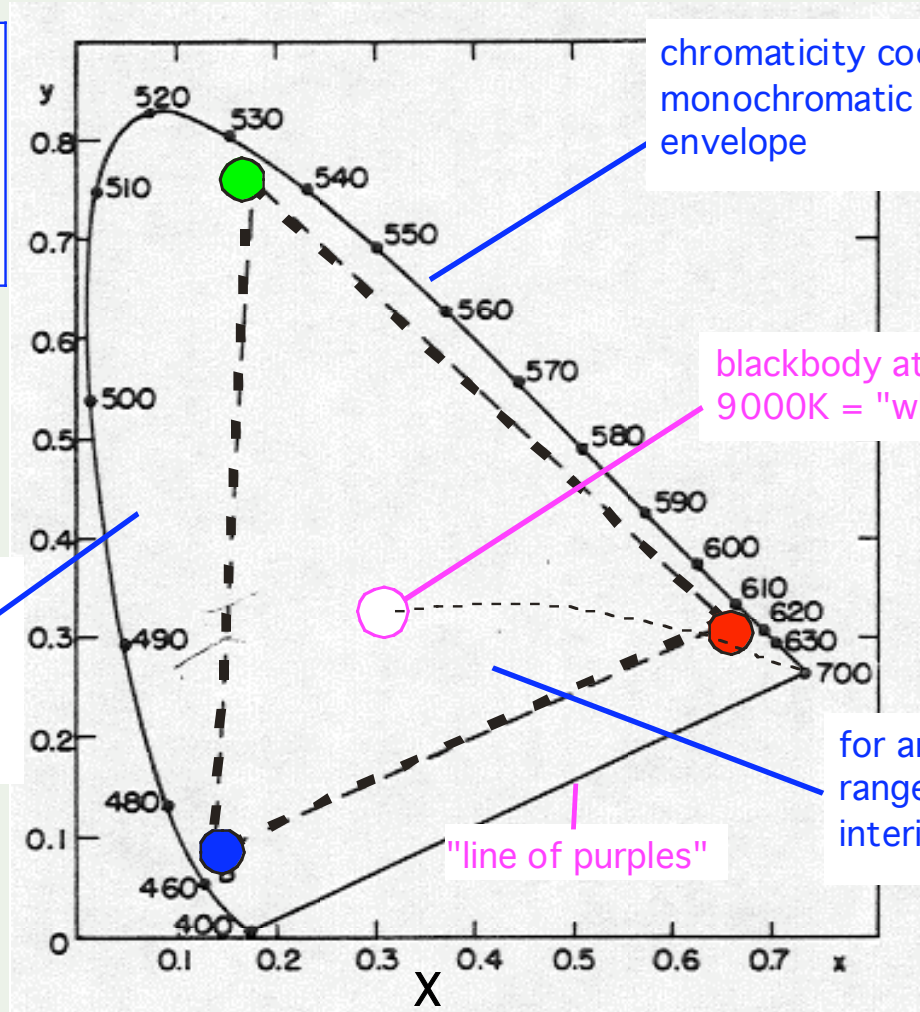
$$y = \frac{Y}{X + Y + Z}$$

$$z = \frac{Z}{X + Y + Z}$$

Result: Chromaticity Diagram

Linear model:
visual sensation of
adding two colors lies
on line between them
on the chart

all visible colors are
made of monochro-
matic colors = inside
envelope



chromaticity coordinates of
monochromatic colors form
envelope

blackbody at 6000-
9000K = "white"

for any given set of "primaries",
range of accessible colors =
interior of triangle

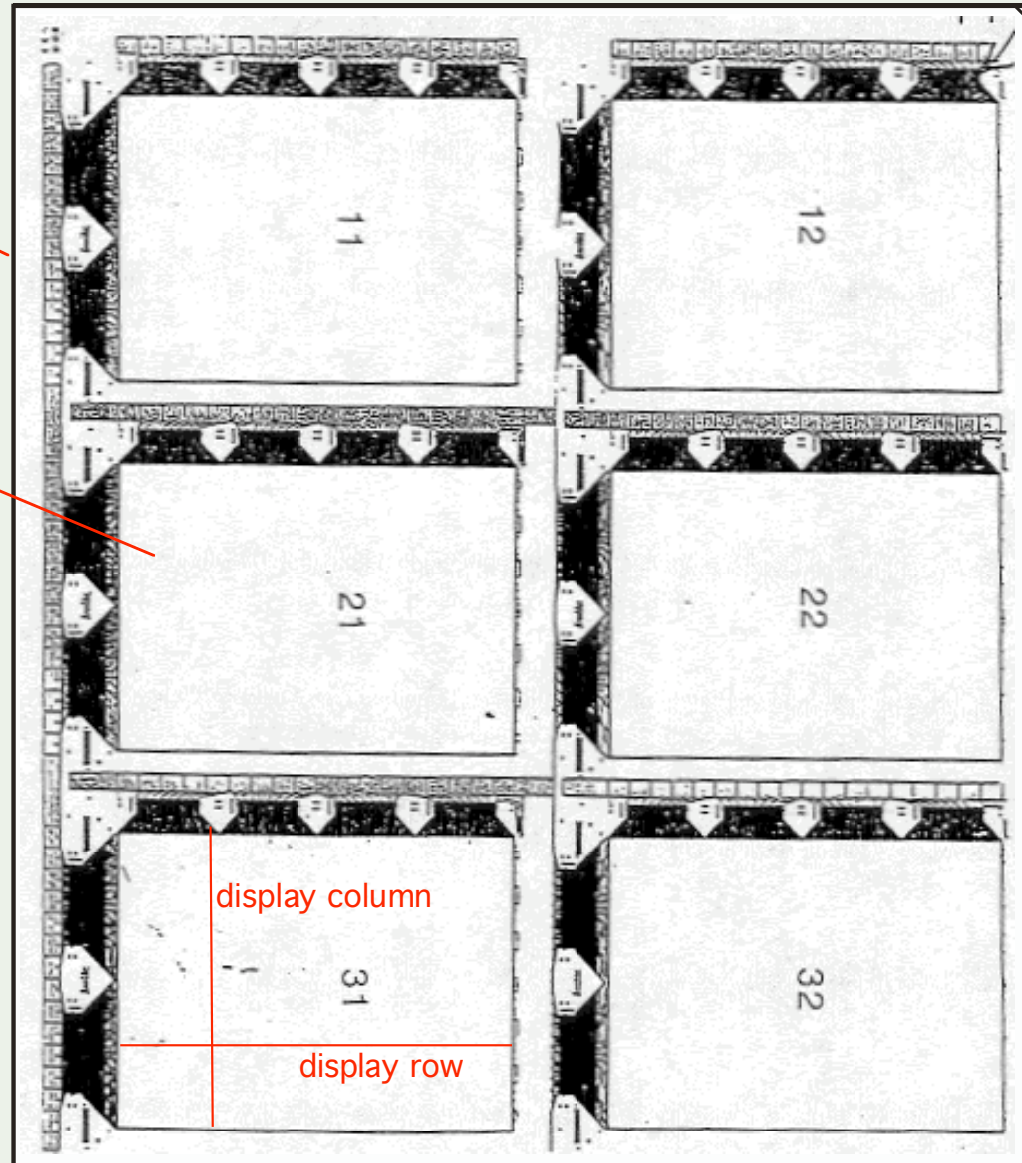
"line of purples"

since $x + y + z = 1$ only need
2 axes (=brightness arbitrary)

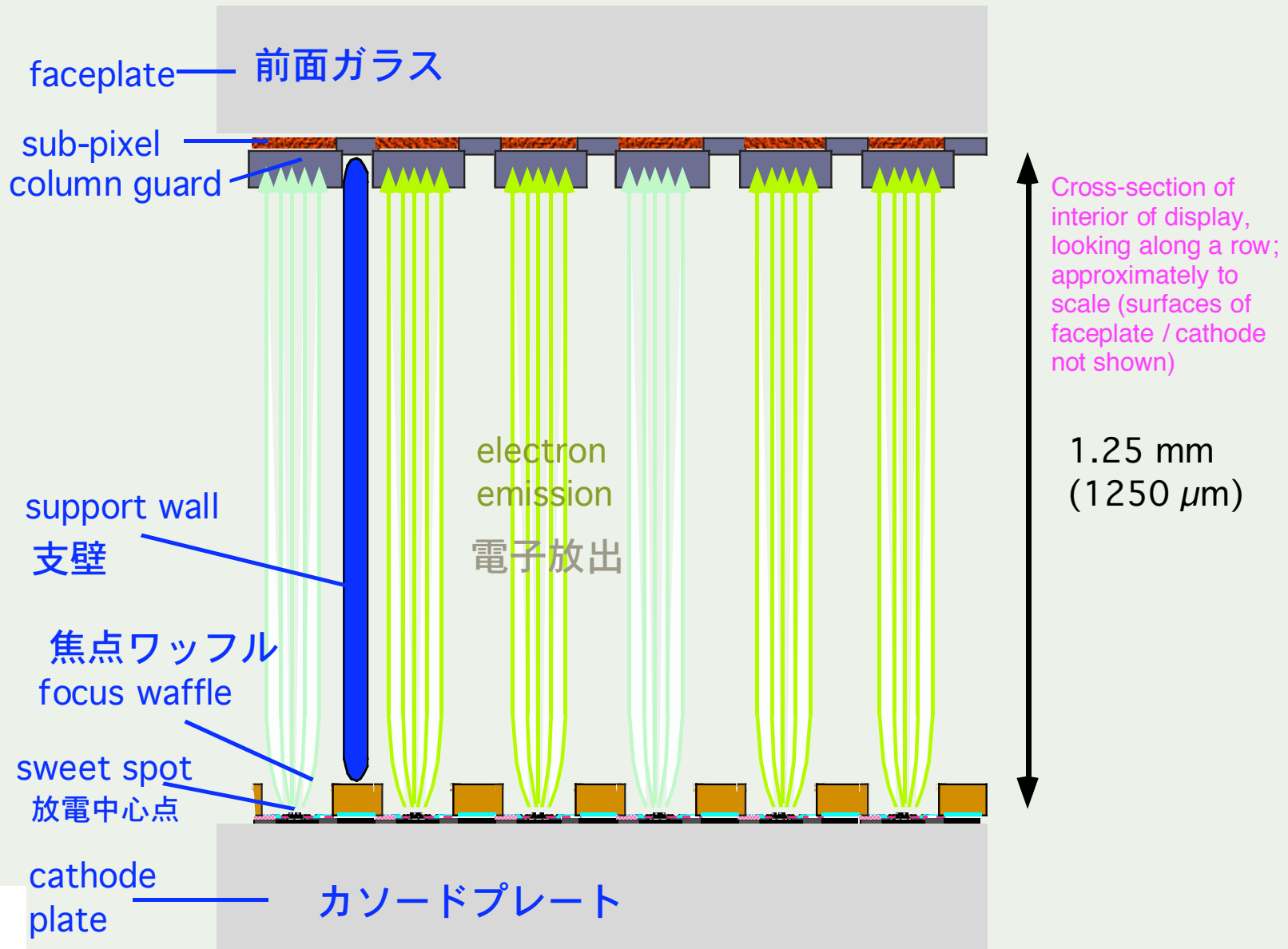
FED Fabrication: Panels and Displays

panel
(340 x 320 mm)

FED display
5.3" [134 mm]
diagonal



Cross-Section of Display



Cathode Overview

- Function: supply controlled electron packets to sub-pixels on the faceplate
- Emission spot: several thousand individual emitters per sub-pixel
- Focus waffle: prevent mixing between neighboring sub-pixels
- Resistive ballasting for emitters: improves uniformity of emission current over the emitters in an emission spot

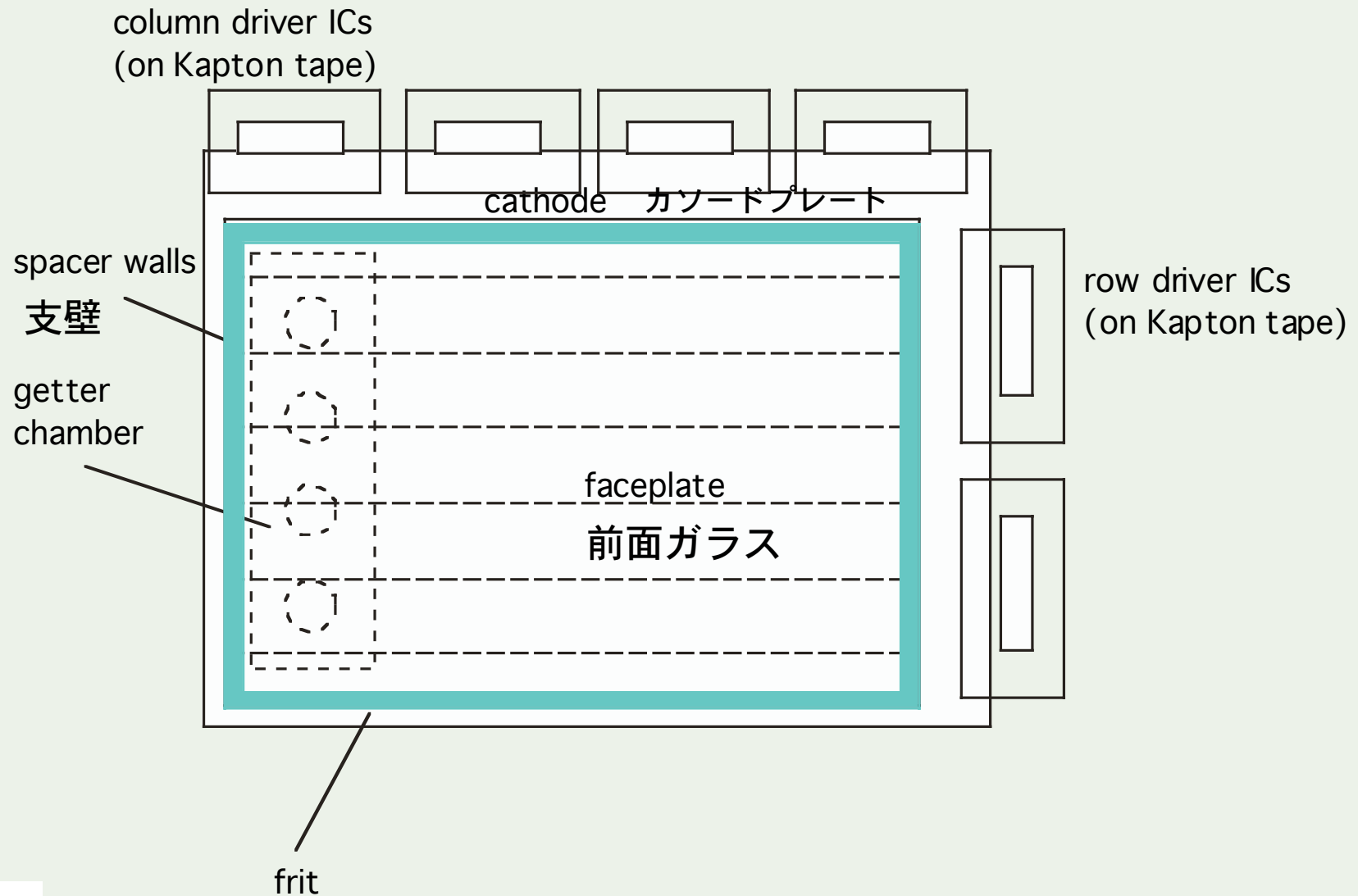
Faceplate overview

- Function: glow in response to electron impact
- Phosphor: aluminized to control charging, reduce ambient reflection
- Pixel: columns of red/green/blue sub-pixels form rows of square pixels
- Column / row guard bands form 'black matrix', about 50 μm high
 - separates pixels
 - suppresses reflection of ambient light

Assembly Overview

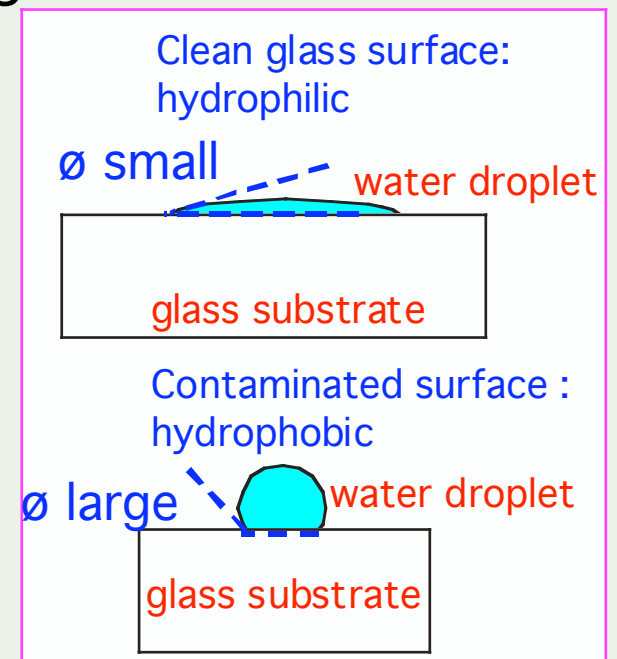
- **Alignment:**
 - assemble cathode and faceplate together so that each emission spot aligns with sub-pixel
- **Spacer walls:**
 - ceramic, 1.2 mm high, 50 microns wide (!)
- **Frit:**
 - fusible Pb-based glass bonds cathode to faceplate
- **Getter:**
 - attached smaller chamber with flash getter to improve vacuum
- **Driver electronics:**
 - attached to periphery
- **Pump down:**
 - 10^{-7} Torr (10^{-5} Pa) needed for reasonable lifetime

Assembled Display



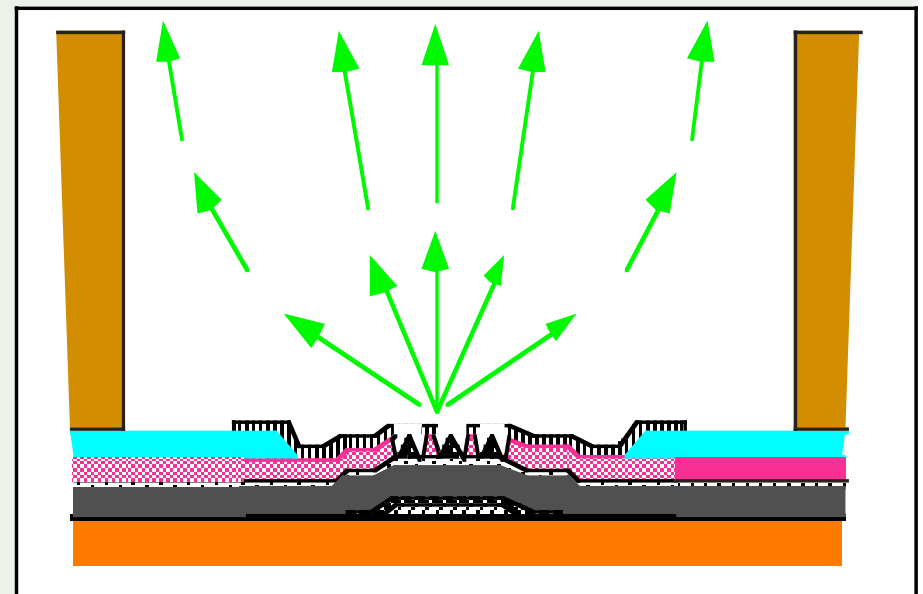
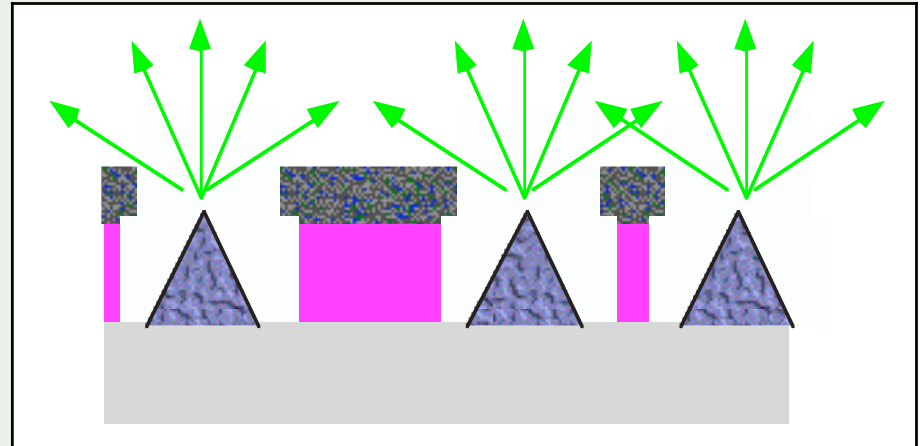
Cathode Parts: Substrate

- Borosilicate glass, e.g. Schott D263
 - identical for cathode and faceplate
 - coefficient of thermal expansion (7 ppm/K) matches that of frit material
 - edges of panel rounded to avoid chips; one corner notched for orientation
 - density at 548°C prior to processing to avoid shrinkage
 - note $T_g=557\text{ }^\circ\text{C}$; support panel to avoid sagging
 - after densification, expect $< 7\text{ }\mu\text{m}$ shrinkage across panel (vs. emission spot size of about $35\text{ }\mu\text{m}$)
 - monitor wetting angle to check for contamination before / after densification
 - particle control critical to prevent row/column shorts



Cathode: Emitters and Focussing

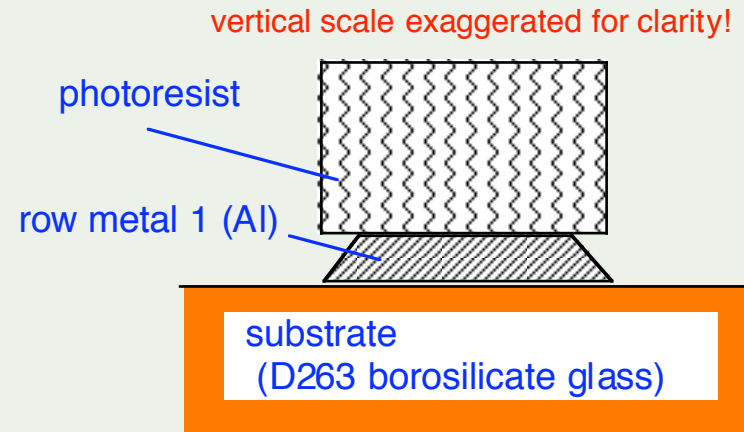
- Individual emitters emit electrons over wide angle
 - color mixing will result for high-voltage FED due to large cathode-faceplate spacing
- Solution: provide focus structure for emission spot
 - thick polyimide + metallization



Cathode Processing: Row metal

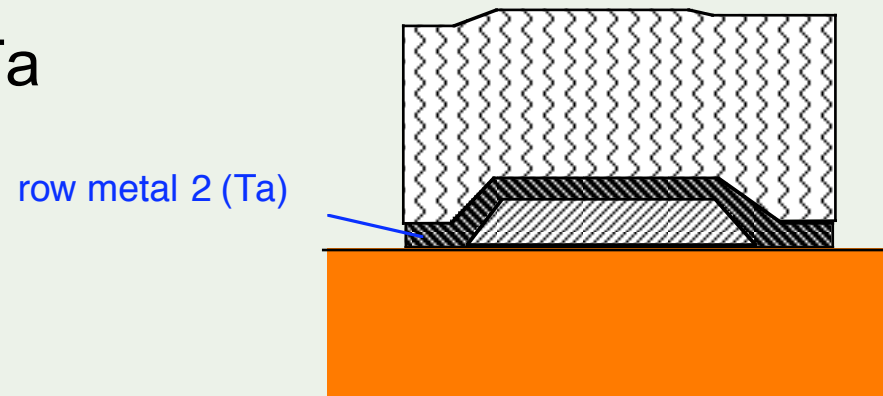
■ Row metal 1:

- sputter & pattern 150 nm Al
 - ensure sloped edge to allow crossovers by column metal



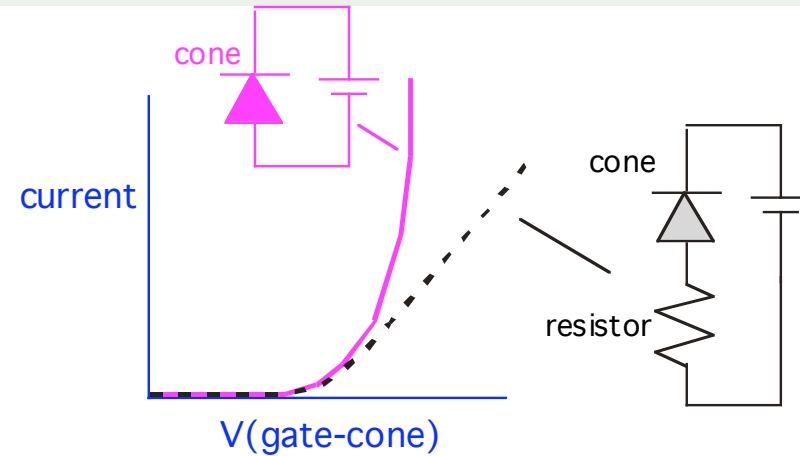
■ Row metal 2:

- sputter & pattern 120 nm Ta
 - hillock prevention, protects Al from corrosive chemicals

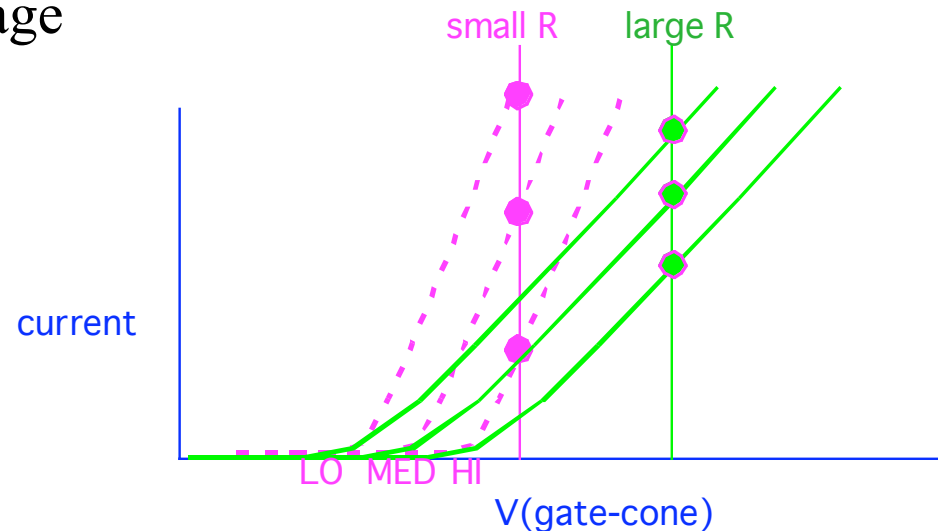
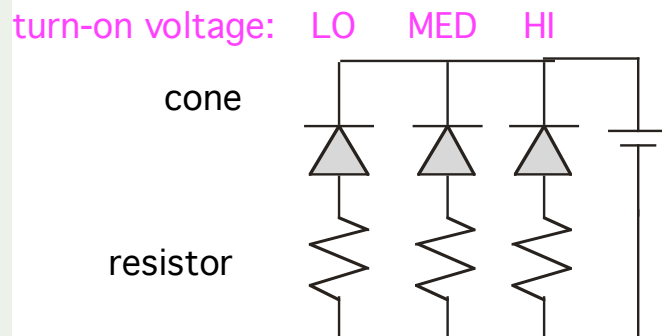


Cathode processing: Resistor Layer

Resistor limits rapid turnon of cones

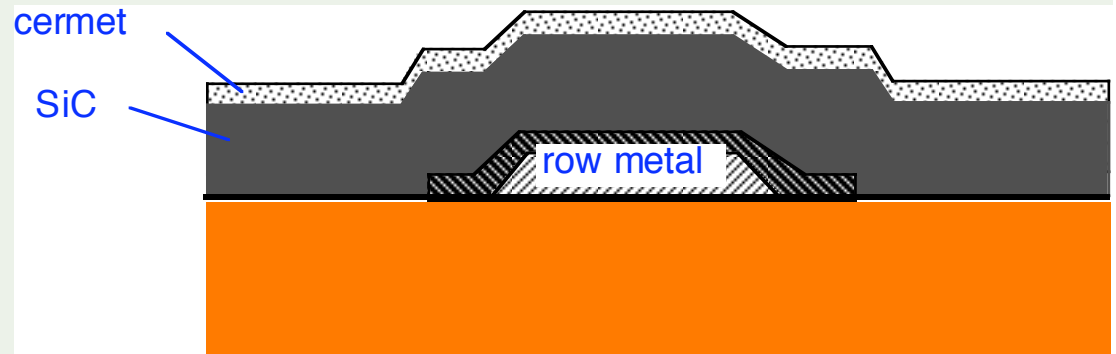


Choice of resistor value is a tradeoff between current uniformity and operating voltage

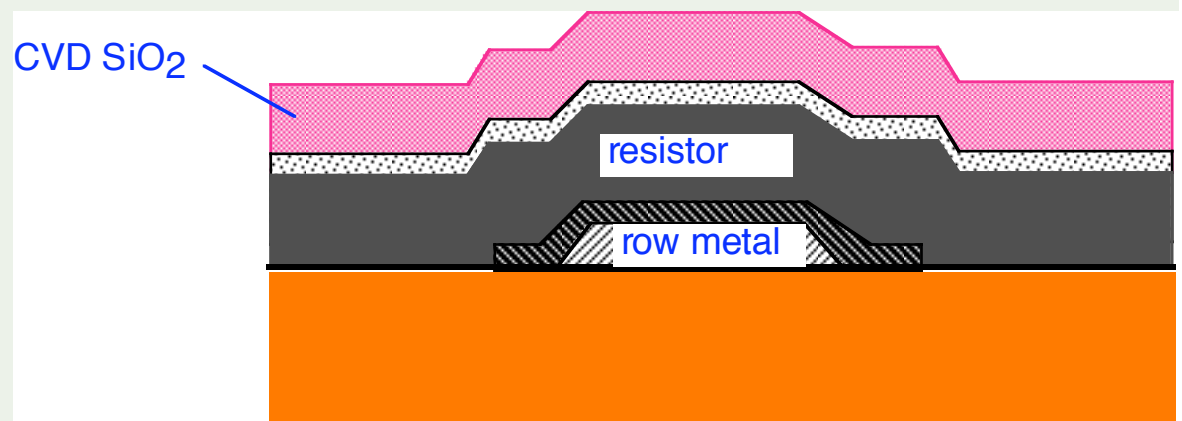


Cathode processing: Resistor layer fab

- 300 nm SiC layer has well-controlled resistivity of about 300,000 Ω -cm
 - series resistance of several G Ω per emitter => about 2 V drop
 - Fused SiC target by CVD, very expensive
 - Material spalls from shields, high particle count
- CVD insulator layer
 - row-column metal insulator
 - gate - emitter insulator
 - 150 nm APCVD (conveyorized belt furnace)
 - shorts represent important yield limiter

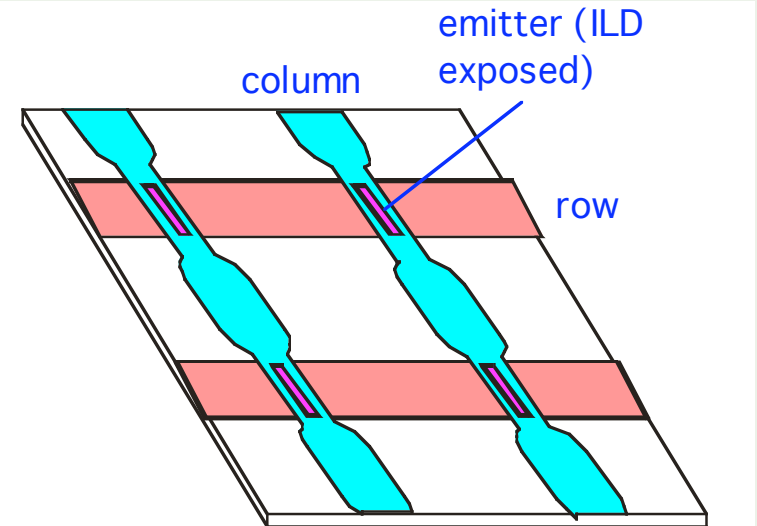
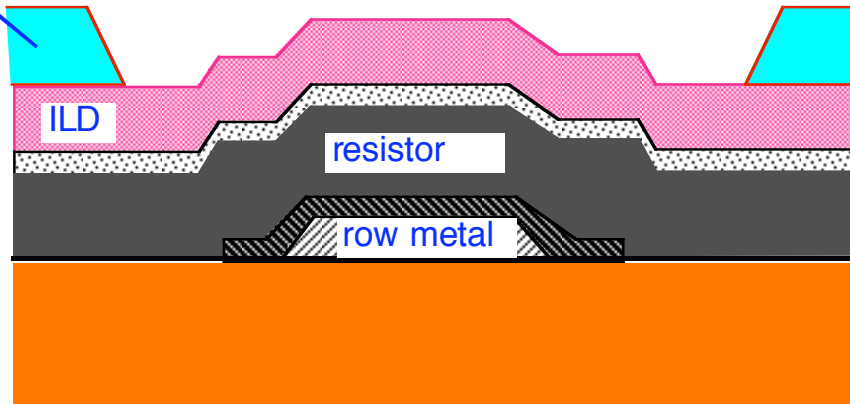


- 50 nm 'cermet' (40% Cr in SiO₂)
 - used as selective etch mask later



Cathode Processing: Column metal

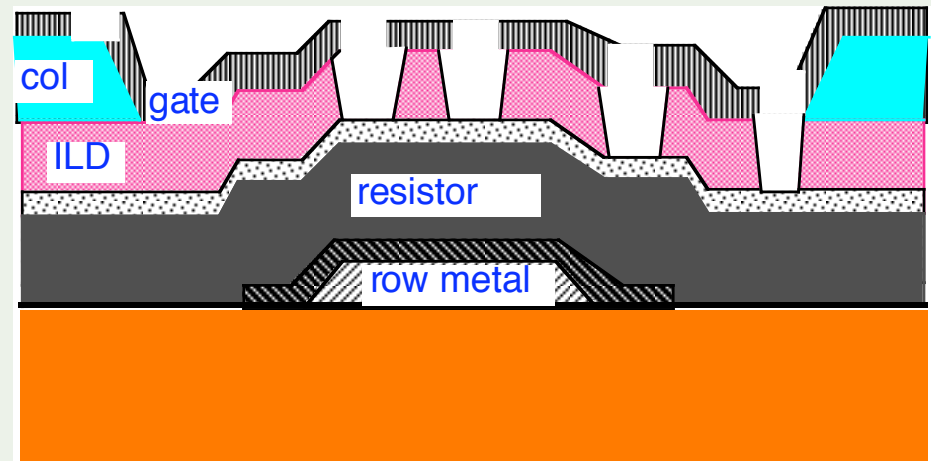
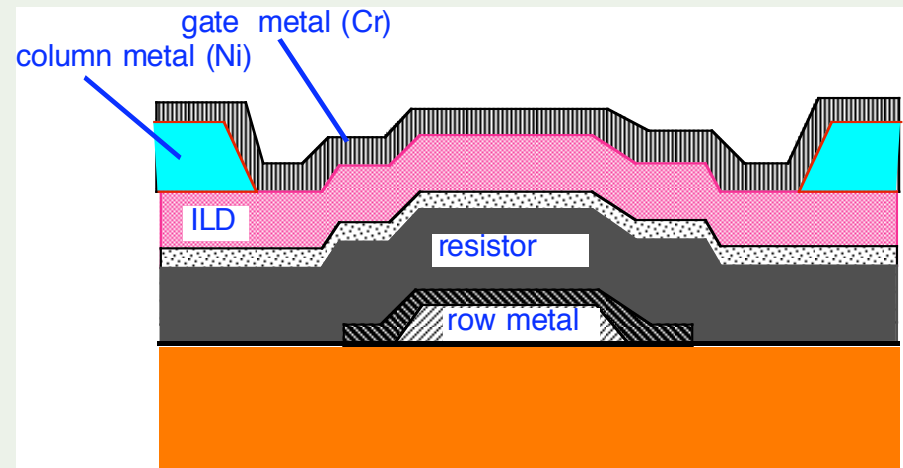
column metal (Ni)



- 150 nm sputtered Ni; wet pattern, sloped edges for contact to gate metal
- Hole in row metal defines emitter region

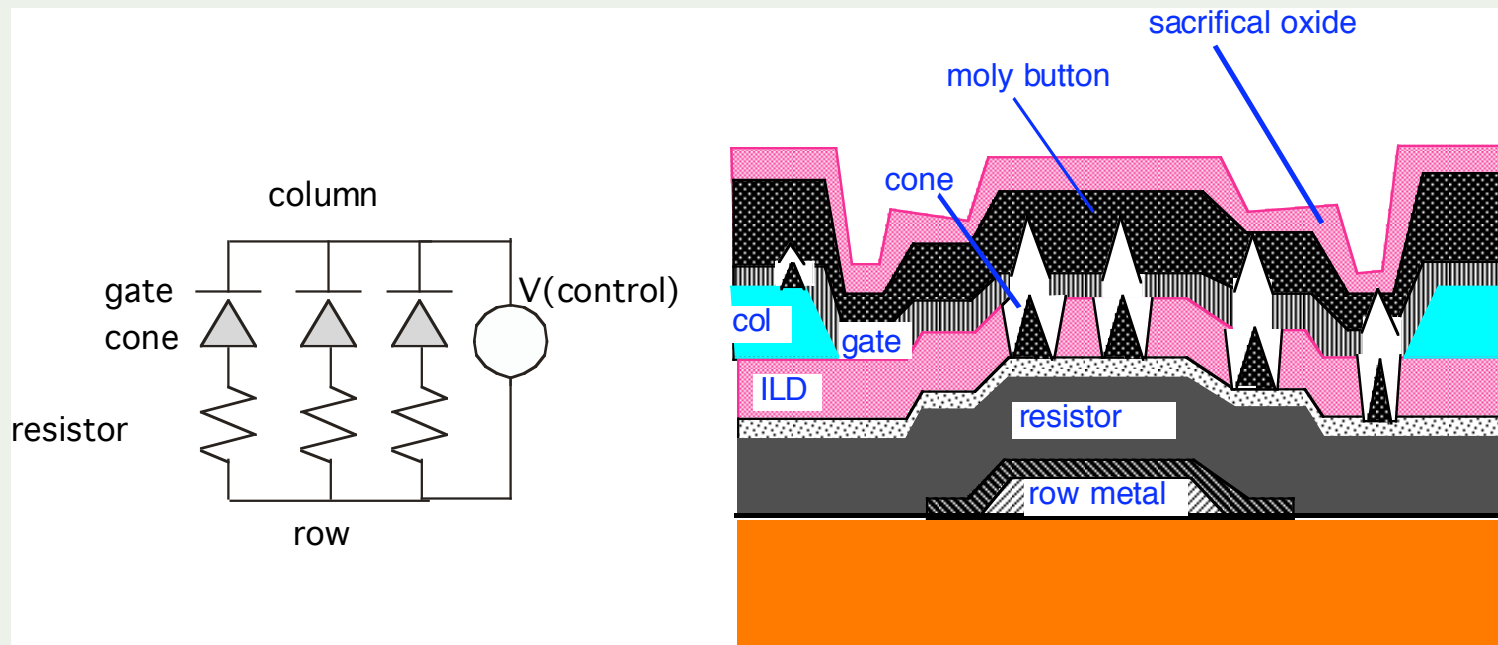
Cathode Processing: Gate metal

- 40 nm Cr masks cavities for discrete emitters
- Pattern and etch



Cathode processing: emitter formation

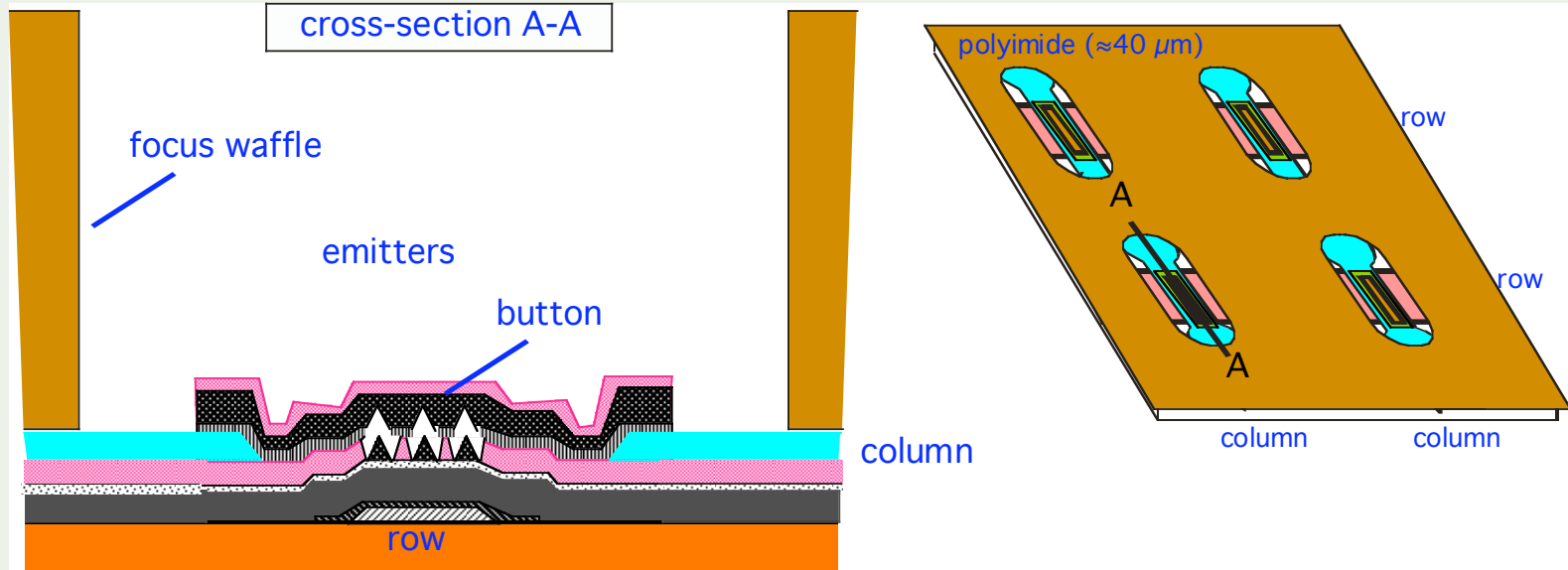
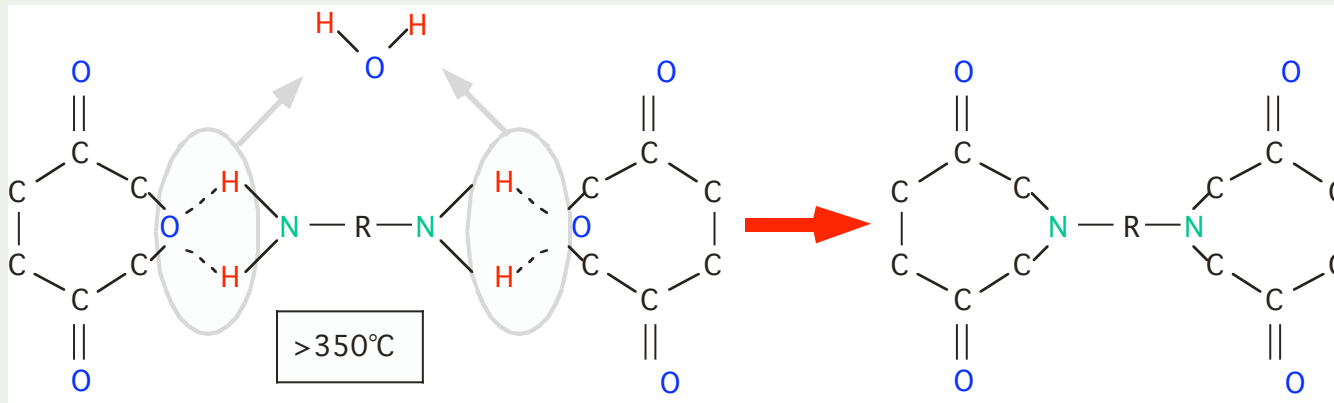
- Spindt cathode (evaporated Mo)
- cover with APCVD SiO_2 afterwards to protect tips during processing



- etch Mo and Cr away except in emitter regions
- etch dielectric to expose row metal

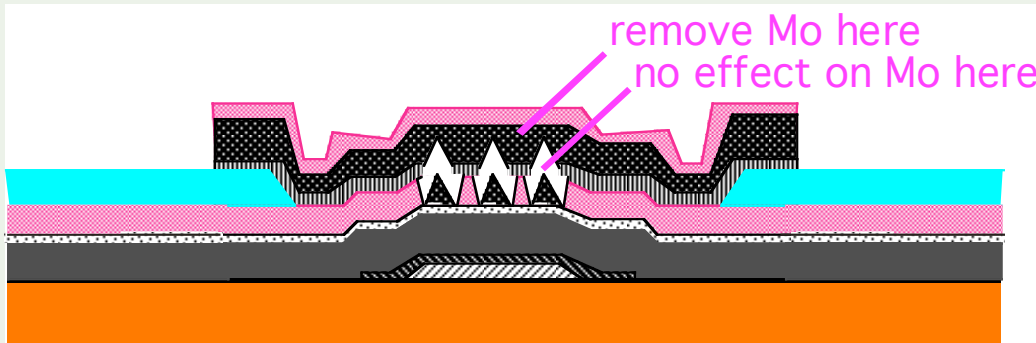
Cathode processing: focus waffle

- Thick (70 μm) photosensitive polyimide, applied while Cr/Mo remains over emitter tips
- Cure 400° C 8 hours in nitrogen after develop

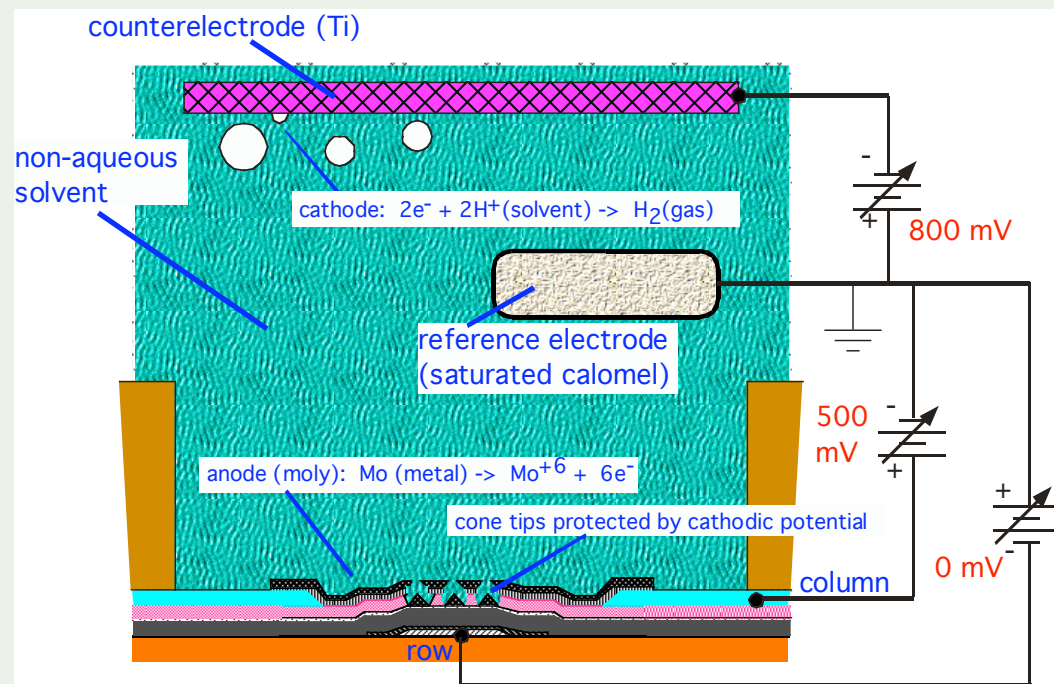


Cathode processing: selective Mo etch

- Challenge: remove Mo 'button' protecting emitters without attacking emitters

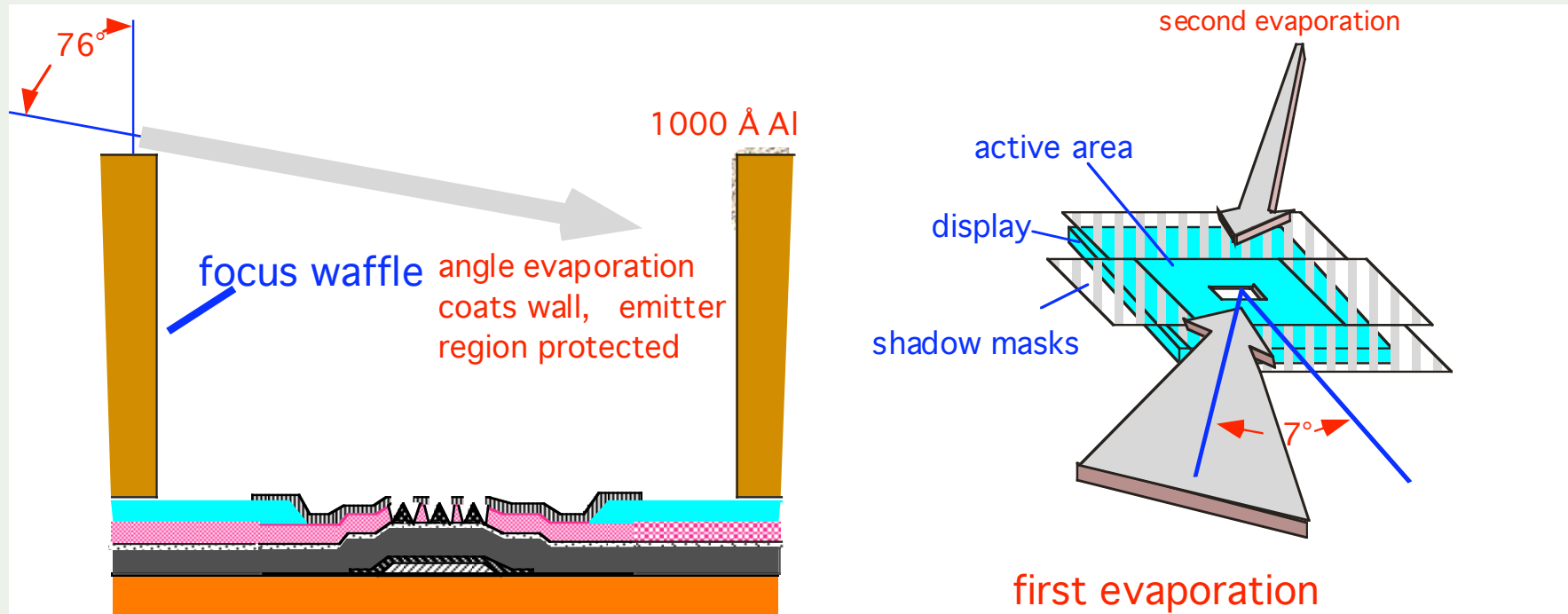


- Approach: use electrochemical etch since 'button' is electrically isolated from emitters



Cathode Process: Focus Waffle Metal

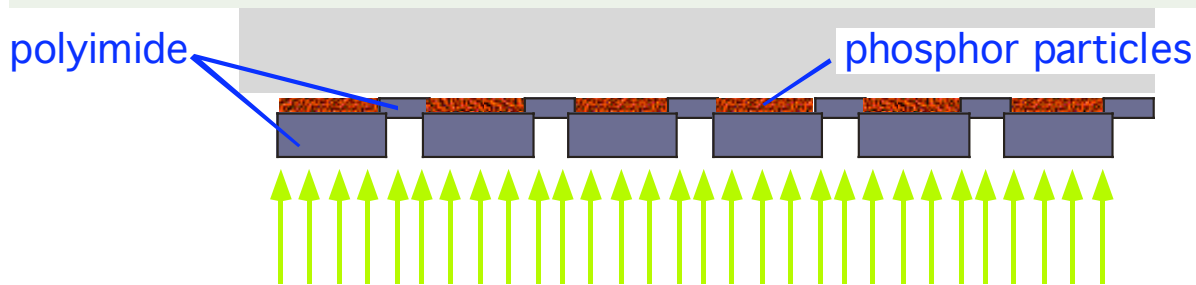
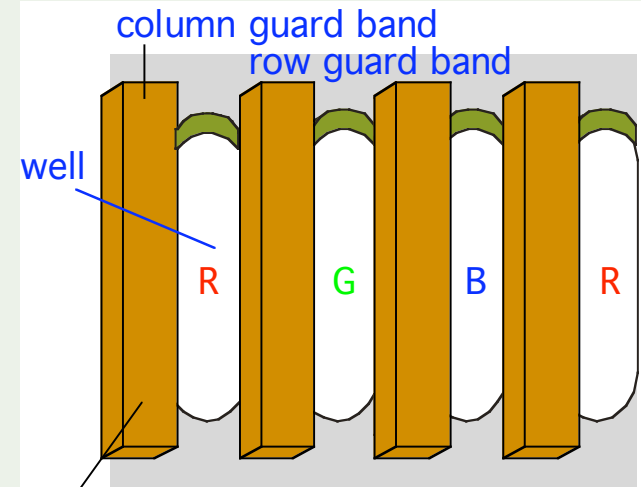
- Use angle evaporation to deposit metal on walls without contaminating emitter region



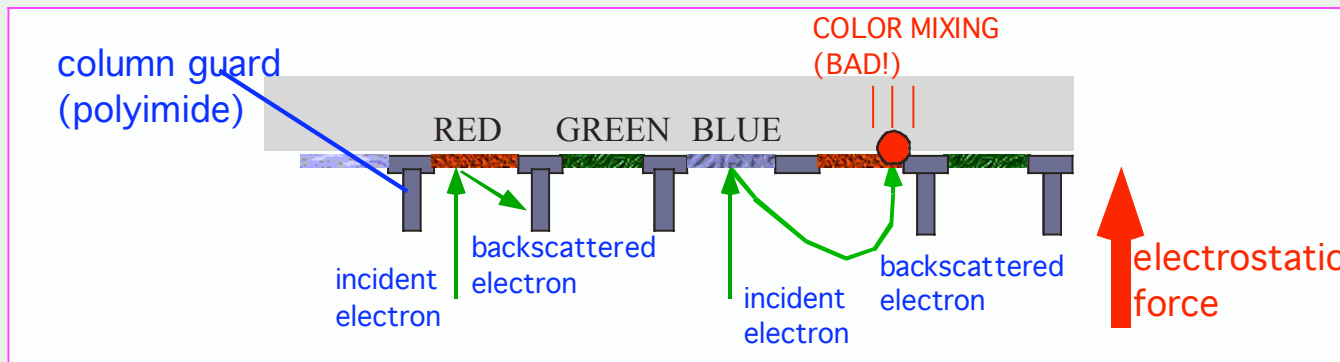
- Ready for bakeout, electrical test, emission uniformity test

Faceplate

- Convert electrons into proper colors
 - thick continuous phosphor films for good color saturation
- Minimize reflection of ambient light
- Minimize scattering of electrons
- Anchor support walls
- Form front of tube

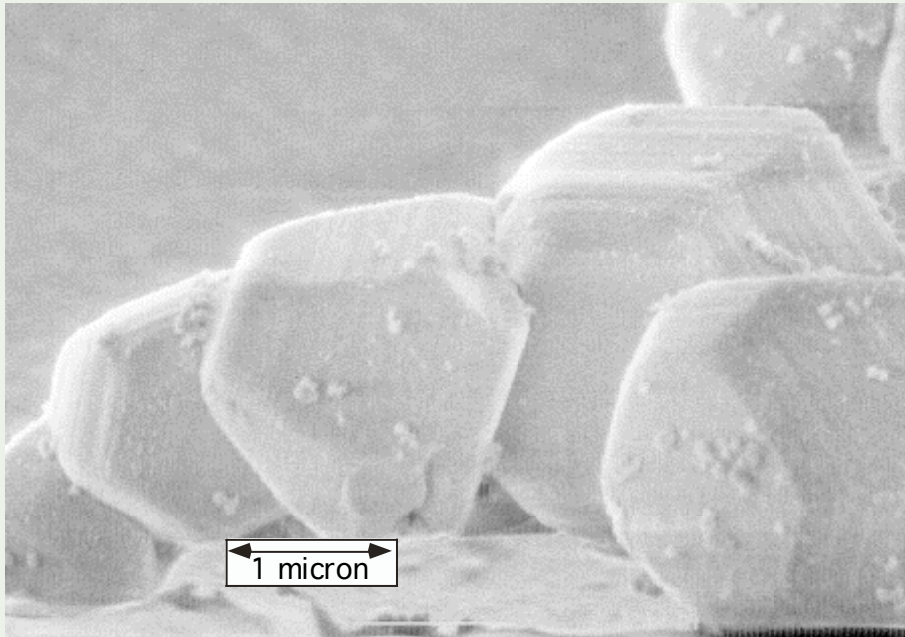


- High-T cure + supercritical extraction to control polyimide outgassing under electron bombardment

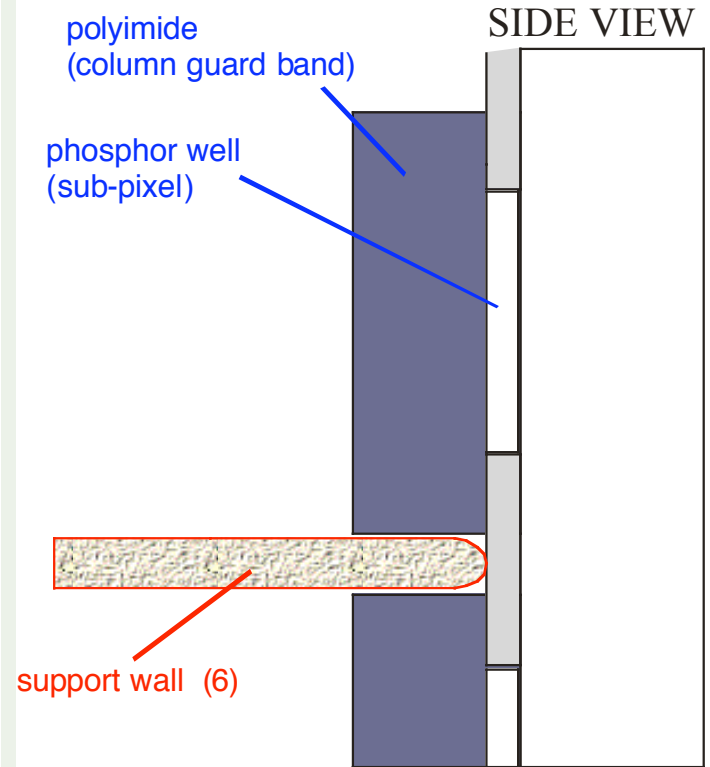
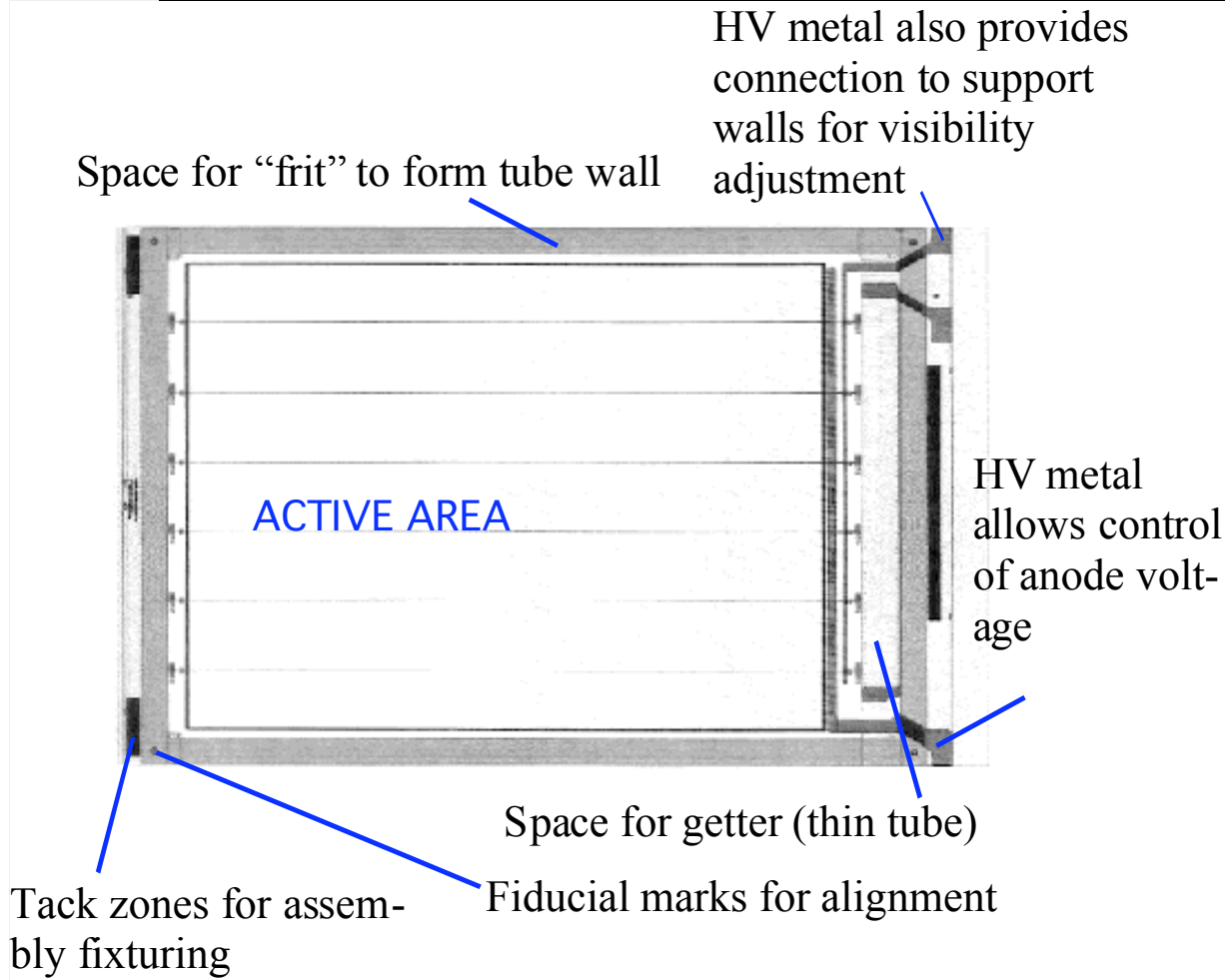


Phosphors

- Typically powders doped with heavy elements
- Typically 2 layers (about 5 μm) thick
- Applied by screen printing from slurry
 - photosensitive slurry + masking to place in correct wells
- Example: 'P22' set:
 - **RED**: yttrium oxysulfide:Eu, medium efficiency
 - **GREEN**: ZnS: Cu/Au/Al, good efficiency
 - **BLUE**: ZnS:Ag/Cl, poor efficiency

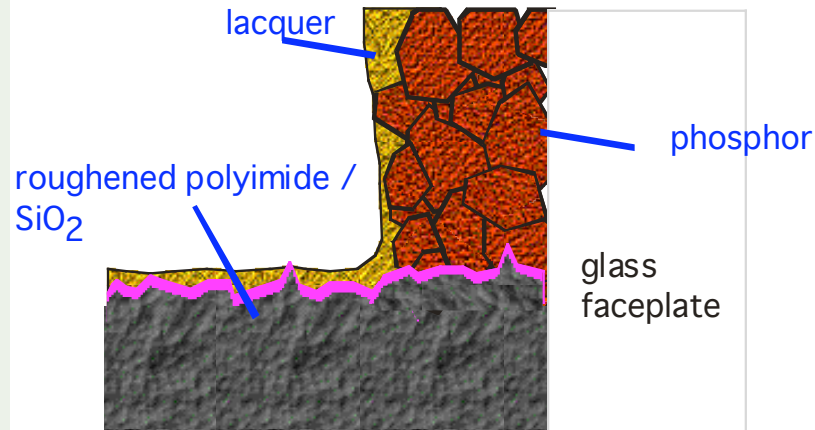


Faceplate Assembly Provisions

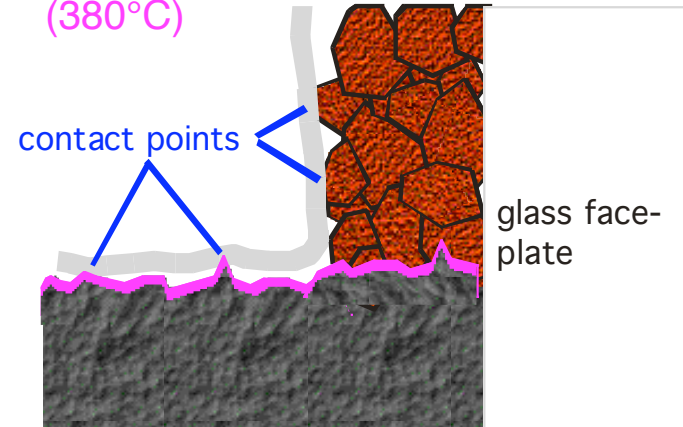


Faceplate: Aluminize

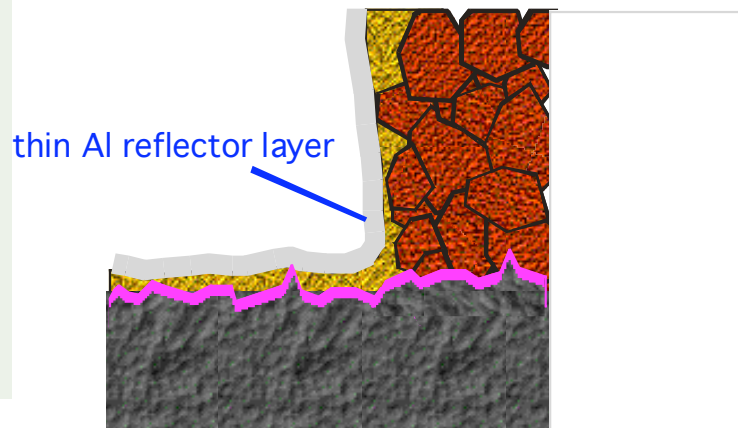
1: Apply lacquer



3: Decompose and remove lacquer (380°C)

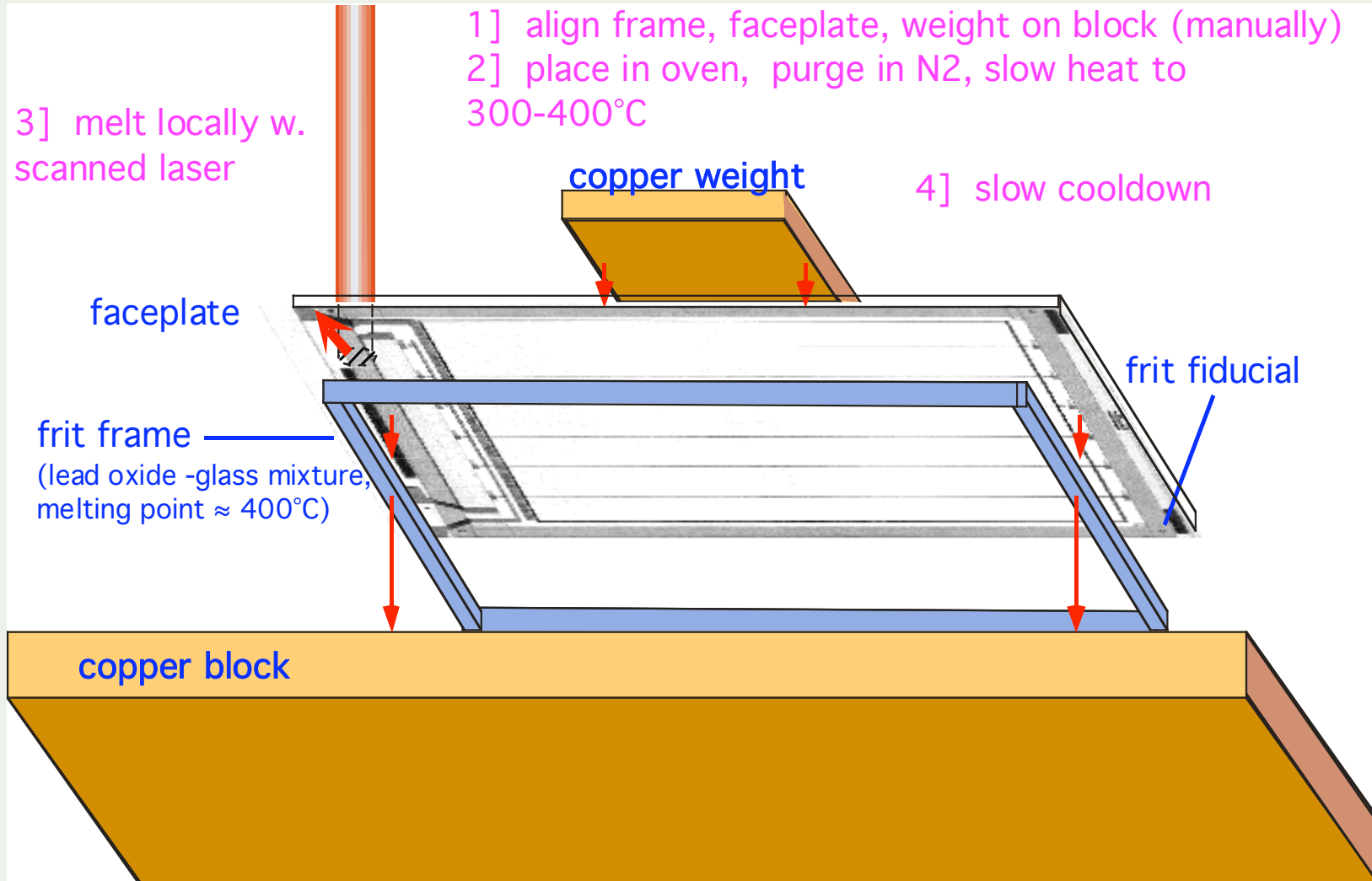


2: Deposit reflector aluminum



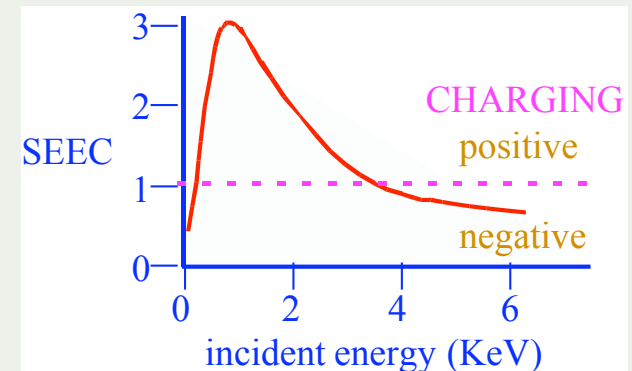
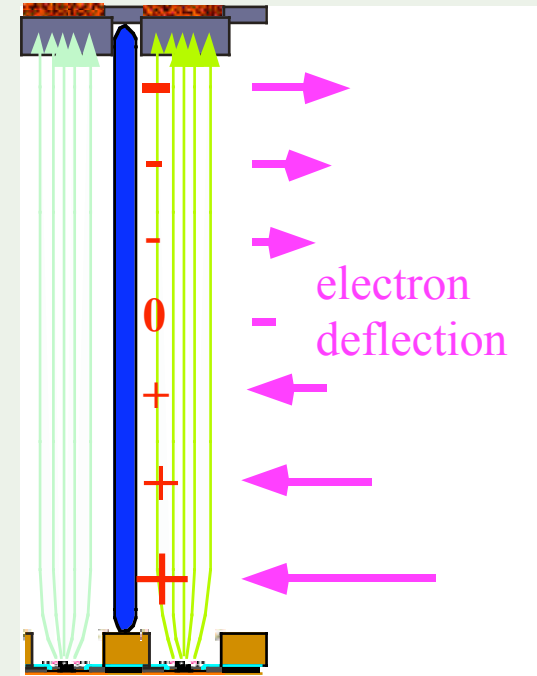
- Minimize emission into tube (lost light)
- Sacrificial lacquer process dates back to 1939

Assembly: Frit Frame Attachment

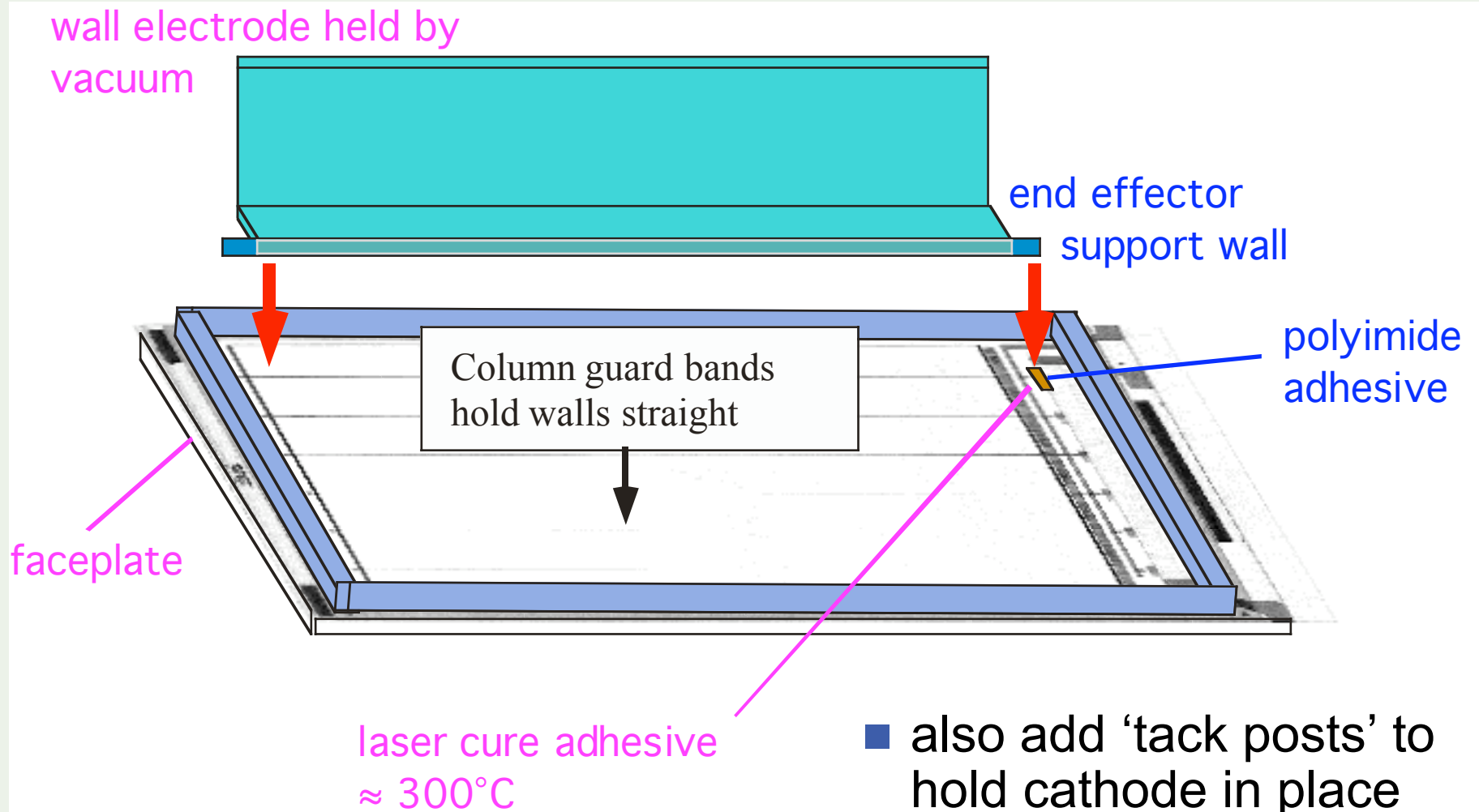


Support Walls

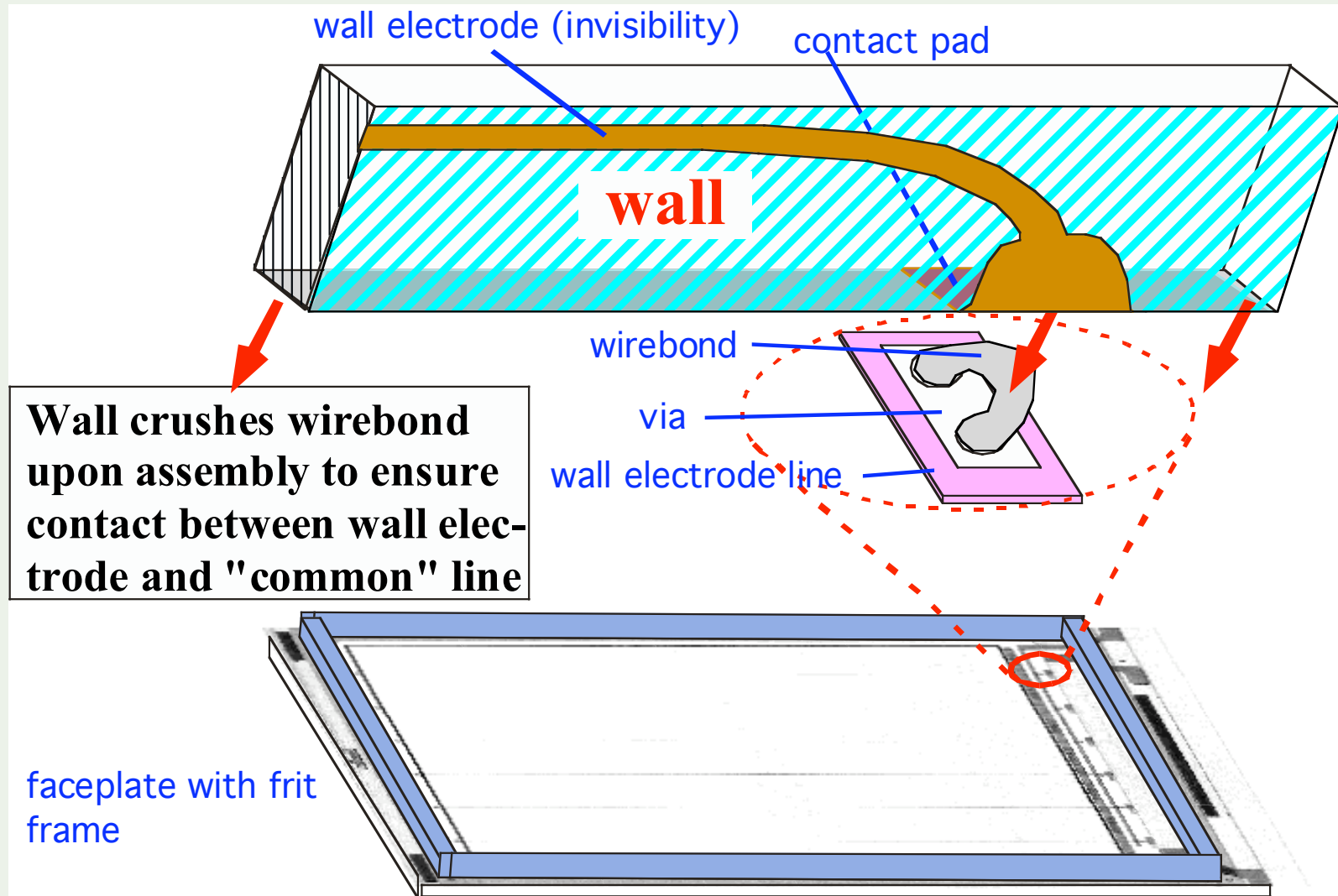
- Charging of support walls due to secondary electron emission deflects electrons, must be controlled
 - coatings, resistivity control
- Mixture of alumina (strength), titania (conductivity), chrome oxide (secondary emission control)



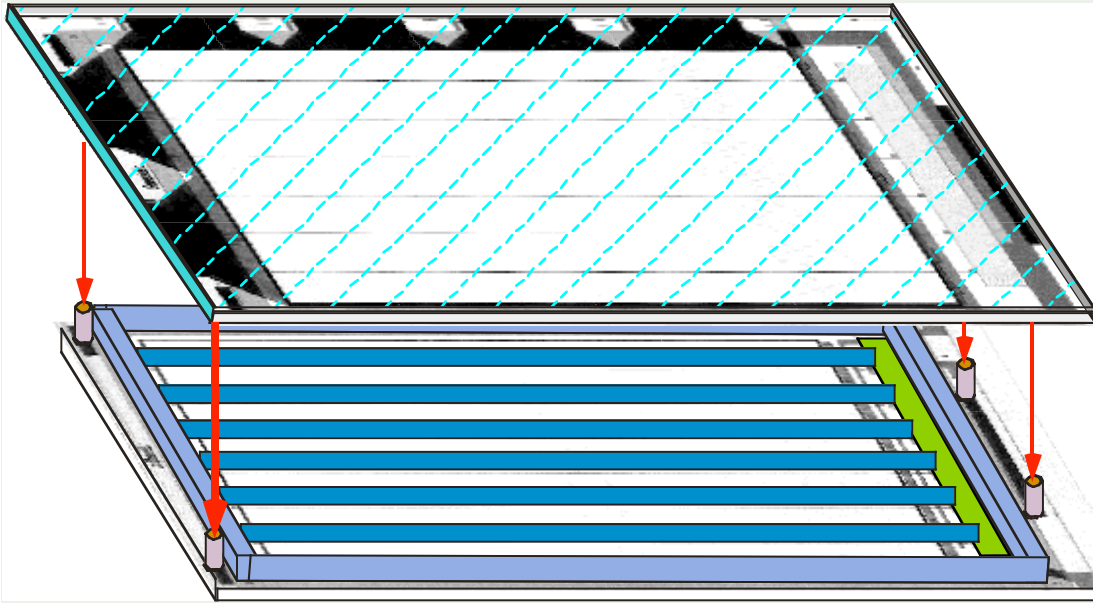
Assembly: Support Walls



Assembly: Wall Electrode Connections

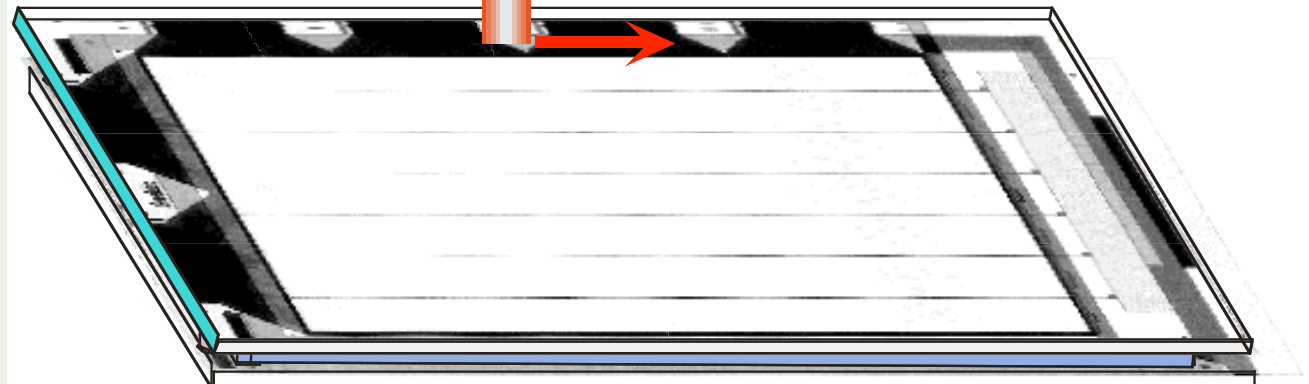


Assembly: Cathode Mount



- part of frit left unsealed to allow pumpout

melt frit locally with laser beam



Assembly: Driver IC's

Kapton tape with
driver IC

anisotropic conduc-
tive adhesive



- and to final test (!)

Conclusions

- Complex display process of which electron emitter is only the first step
- Emitter tolerance of contamination is a critical issue (but not the only one):
 - contamination and damage in processing
 - outgassing during life of display
 - degradation in emission may limit display life
 - Carbon nanotubes should help
- Other problems are catastrophic failure (arcing?) and internal charging:
 - “Nearly all panel failures were of the catastrophic variety, even with ...careful derating of the accelerating voltage. I consider the high voltage holdoff, combined with the need for structures that remain absolutely neutrally charged despite variable electron flux, to be the killer problem(s) for this technology.” --Stephanie Oberg, formerly with Candescent
 - These problems are not addressed by substitution of carbon nanotubes for Spindt cathodes

Acknowledgments

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